CN9130 SOM

SolidRun Ltd.

Revision History

Rev#	Date	Owner	Description
1.0	Jan 2021	AlonR	First Release
1.1	June 2021	AlonR	1. Fix DDR bus width BUG 2. Update MPPs to support RGMII CP_GE2 3. Fix RGMII 1.8V support with CP_VDDO A & D 4. Correct EEPROM address to 0x53 5. changed EFUSE due to stock shortage 6. changed 1.2V DC-DC due to stock shortage 7. Removed MCU 8. Changed SPI MUX
1.3	Jan 2023	AlonR	1. Move components in layout that colide with the mating connector on the carrier 2. add termination on ECC DQ[3:0]. DQS and DM 3. changed C99 to 10uF 4. removed C115

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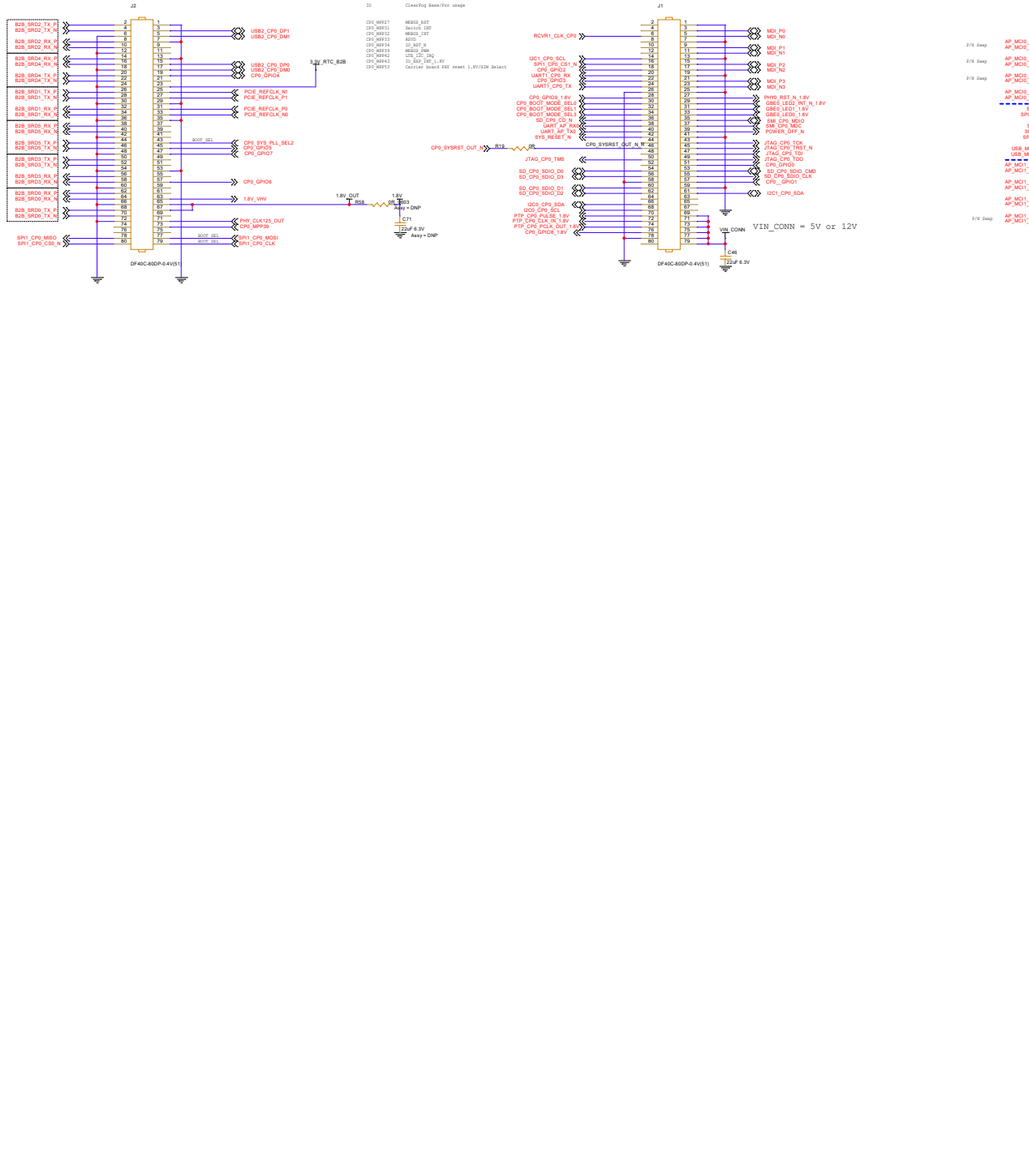
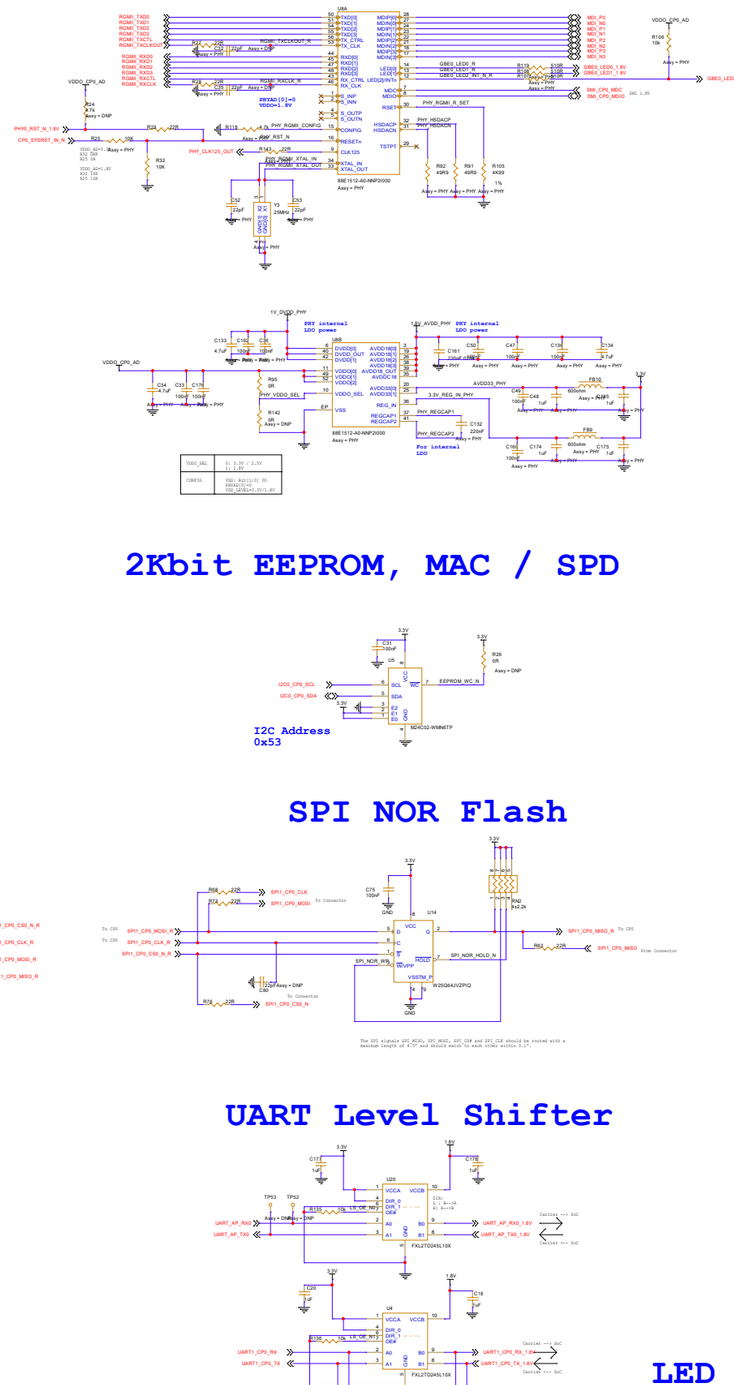
SOM Conn A/B/C

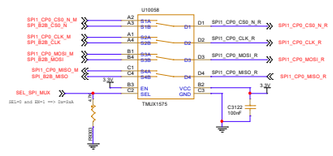


1GbE PHY



2Kbit EEPROM, MAC / SPD

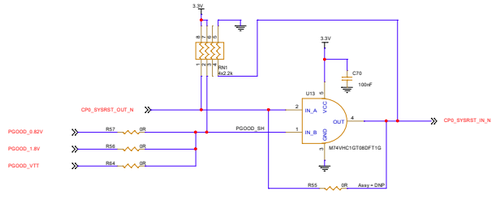
SPI MUX



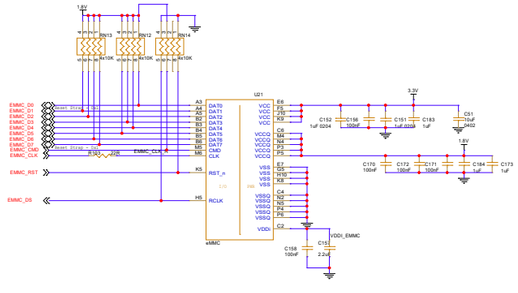
SPI NOR Flash

UART Level Shifter

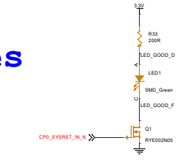
RESET Circuit



eMMC



LED



Mechanical Holes

SolidRun			
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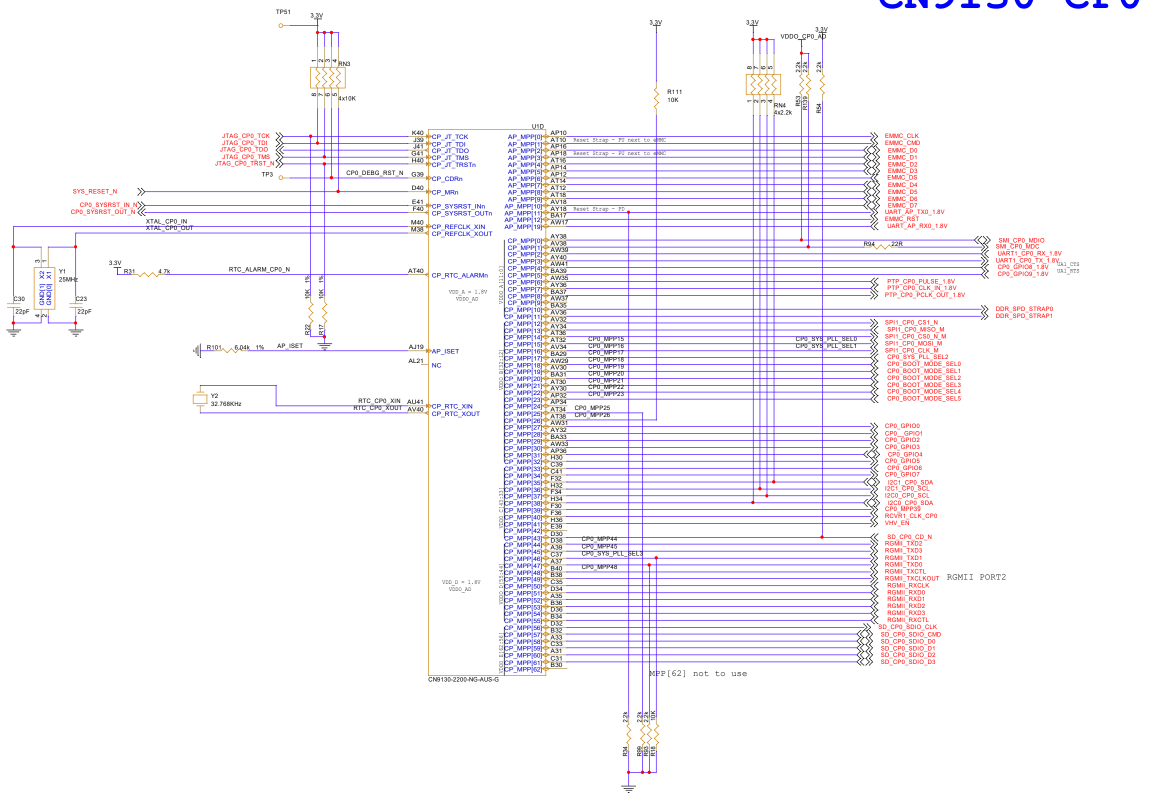
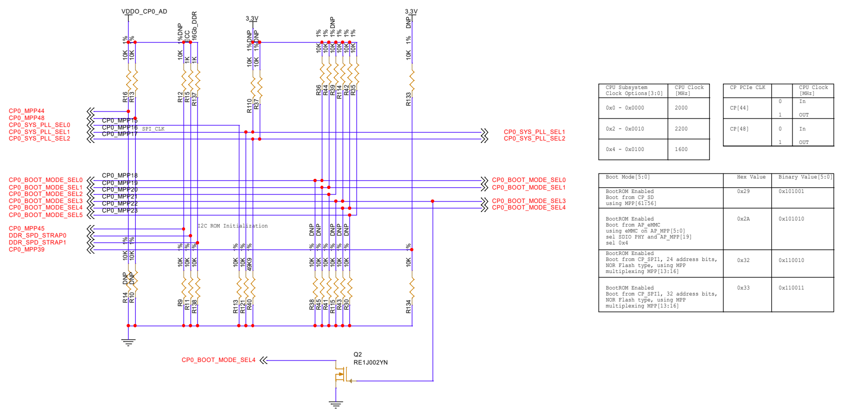
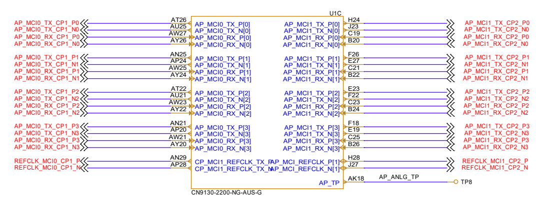
CN9130 CP0 MPPs



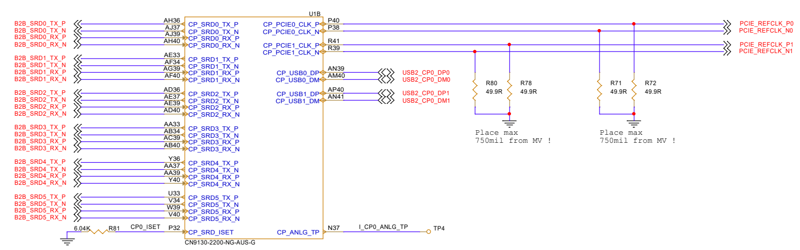
CP0 Boot Straps



CN9130 MoCi



CN9130 SERDES



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