

CN9130 SOM

SolidRun Ltd.

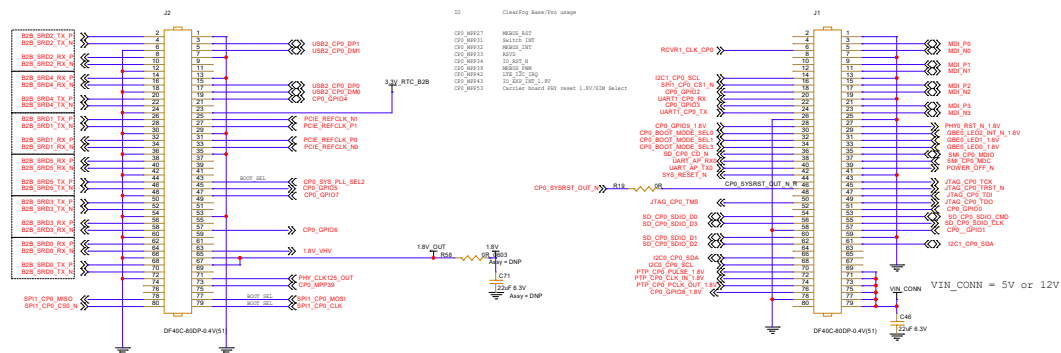
Revision History

Rev#	Date	Owner	Description
1.0	Jan 2021	AlonR	First Release
1.1	June 2021	AlonR	1. Fix DDR bus width BUG 2. Update MPPs to support RGMII CP_GE2 3. Fix RGMII 1.8V support with CP_VDDO A & D 4. Correct EEPROM address to 0x53 5. changed EPFUSE due to stock shortage 6. changed 1.2V DC-DC due to stock shortage 7. Removed MCU 8. Changed SPI MUX
1.3	Jan 2023	AlonR	1. Move components in layout that colide with the mating connector on the carrier 2. add termination on ECC DQ[3:0], DQS and DM 3. changed C99 to 10uF 4. removed C115

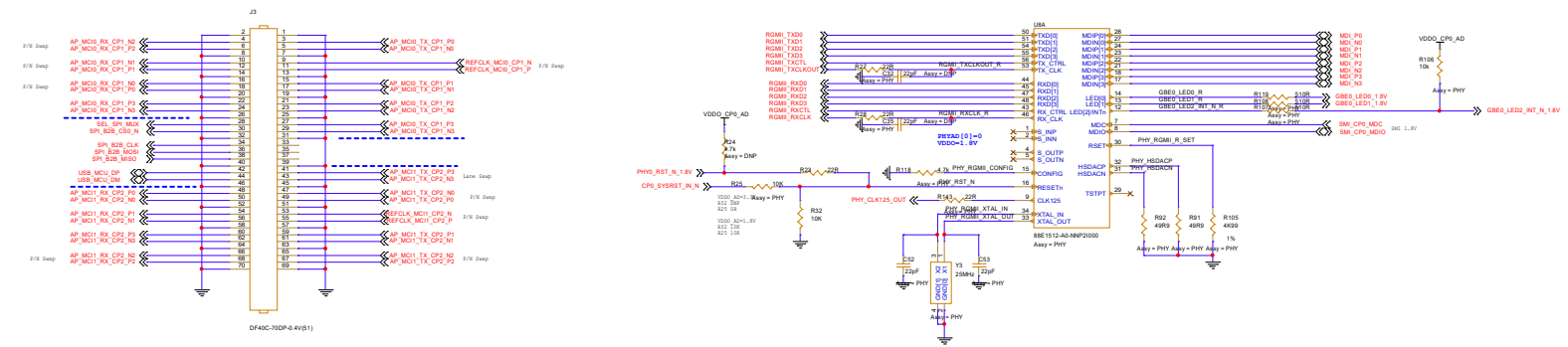
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1	B2B DC-DC Perph	Board to board connectors, MISC and power blocks
2	Processor	MPPs, CPU Power, GND and SERDESs

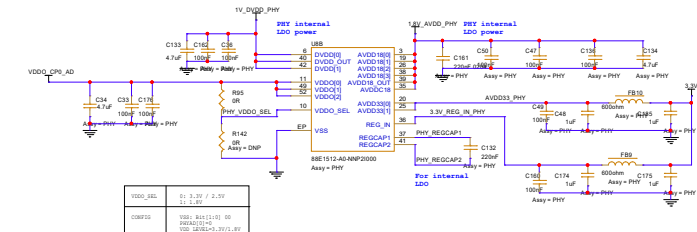
SOM Conn A/B/C



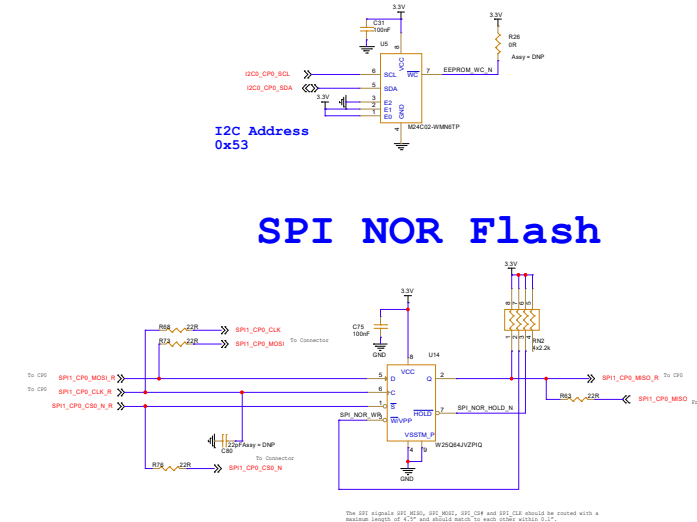
1GbE PHY



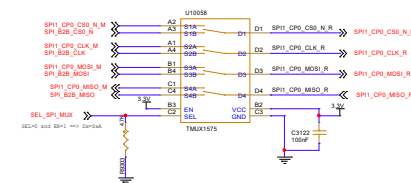
2Kbit EEPROM, MAC / SPD



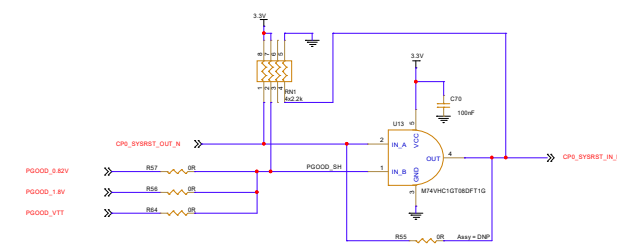
SPI NOR Flash



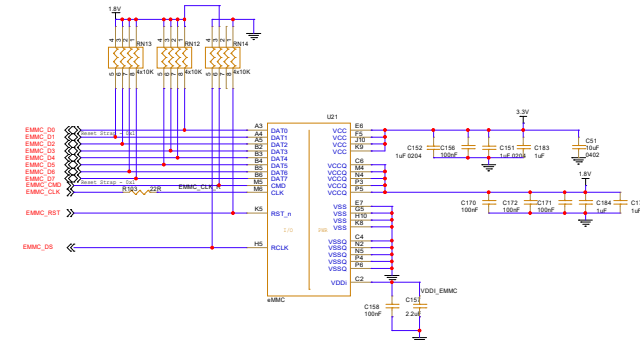
SPI MUX



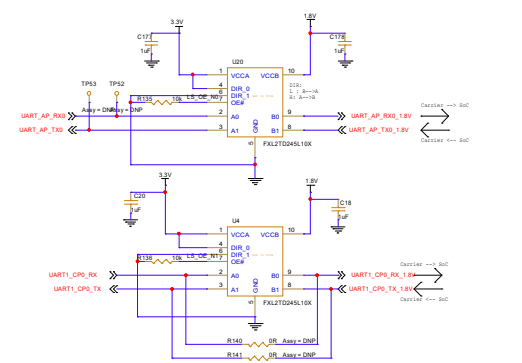
RESET Circuit



eMMC



UART Level Shifter



Mechanical Holes



LED



CP0 Boot Straps

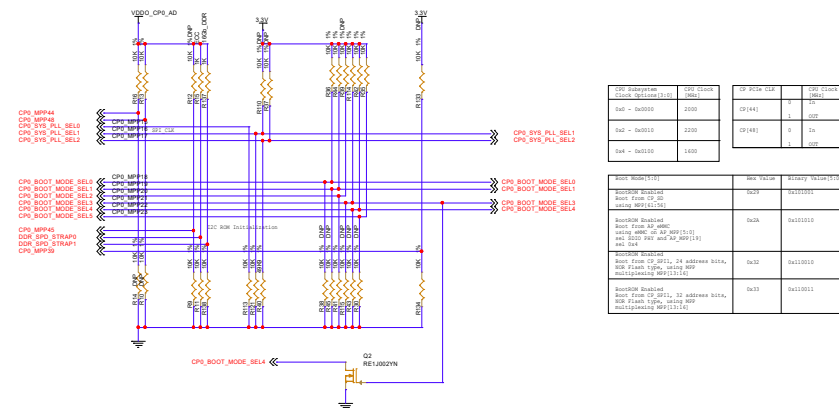


Figure 1 is a schematic representation of the 128-bit data path of the proposed architecture. The diagram shows a 128-bit data path with 128 input registers (AP, MP, and REF) and 128 output registers (AP, MP, and REF). The data path is divided into four main sections: AP, MP, REF, and a final output section. Each section contains a series of registers and multiplexers. The AP section has 32 registers, the MP section has 32 registers, and the REF section has 32 registers. The final output section has 32 registers. The data path is controlled by a 128-bit control signal (AP, MP, REF) and a 128-bit output signal (AP, MP, REF). The diagram also shows a 128-bit control signal (AP, MP, REF) and a 128-bit output signal (AP, MP, REF) at the bottom.

[illegible]