SERDES Block

U99 SERDES #2

SD2_RX0_P … SD2_RX7_P / SD2_RX0_N … SD2_RX7_N → SD2_RX0/7 P/N (AW19, AU19, AV20, AT20, AV21, AT21, AV22, AT22, AV23, AT23, AV24, AT24, AV25, AT25, AV26, AT26, AV27, AT27)

SD2_TX0_P … SD2_TX7_P / SD2_TX0_N … SD2_TX7_N → SD2_TX0/7 P/N (AP19, AN19, AP20, AN20, AP21, AN21, AP22, AN22, AP23, AN23, AP24, AN24, AP25, AN25, AP26, AN26, AP27, AN27)

SD2_RX0/7 P/N for LX2160 Only

SD2_TX0/7 P/N for LX2160 Only

SD2_RX0_P … SD2_RX7_P → SD2_TX0_P … SD2_TX7_P

SD2_RX0_N … SD2_RX7_N → SD2_TX0_N … SD2_TX7_N

SLOT1_TX0_P … SLOT1_TX7_P / SLOT1_TX0_N … SLOT1_TX7_N

SATA0_TX_P / SATA0_TX_N

SATA1_TX_P / SATA1_TX_N

SD2_PLL_REF_CLK_P / SD2_PLL_REF_CLK_N

SD2_PLL_TPA / SD2_PLL_TPD

SD2_PLL_TPA / SD2_PLL_TPO

SD2_IMP_CAL_RX / SD2_IMP_CAL_TX

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SD2_RX0_P 200 SD2_IMP_CAL_RX

SD_SVDD_FLT 1.5K SD2_IMP_CAL_TX

SERDES Block

U98 SERDES #3

SD3_RX0_P … SD3_RX7_P / SD3_RX0_N … SD3_RX7_N → SD3_RX0/7 P/N

SD3_TX0_P … SD3_TX7_P / SD3_TX0_N … SD3_TX7_N → SD3_TX0/7 P/N

SD2_RX0/7 & SD2_TX0/7 for LX2160

SD3_PLL_REF_CLK_P / SD3_PLL_REF_CLK_N

SD3_PLL_TPA / SD3_PLL_TPD

SD3_PLL_TPA / SD3_PLL_TPO

SD3_IMP_CAL_RX / SD3_IMP_CAL_TX

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SD3_RX0_P 200 SD3_IMP_CAL_RX

SD3_SVDD_FLT 1.5K SD3_IMP_CAL_TX

SerDes Protocols Supported

LX2160: 8 - PCIe.3 x8

LX2081: 8@x8 - PCIe.3 x8

SERDES Clocks

SD3CLK_I/O, SD3CLK_VDD, SD3CLK_VDDX, SD3CLK_VDDA

Crystal Load Caps: Crystal: 12 pF; Traces: 3 pF; 1612AH: 4.5 pF; CL = 18 pF

Y1 25MHz

PEXCLK_XTAL1 / PEXCLK_XTAL2

U12 8SLP222B-AG1AGM

XIN_CLKIN, XOUT, VSSR, REF_SA, SD23_REFCLK

DIFF0_P/N … DIFF7_P/N

UCLK_SD2_F_P … UCLK_SD2_H_N

UCLK_SLOT1_F_P … UCLK_SLOT1_H_N

UCLK_SD3_F_P … UCLK_SD3_H_N

SYSCLK_DIFF_P / SYSCLK_DIFF_N

CLK_SD2_F_P … CLK_SD2_H_N

CLK_SLOT1_F_P … CLK_SLOT1_H_N

CLK_SD3_F_P … CLK_SD3_H_N

OE0_B … OE7_B (PD)

SS_EN (PU)

PWRGD/PWRDN_B(PU)

FS (PD)

SDA, SCLK

Share pads

CFG_SPREAD

I2C1_CH1_SDA / I2C1_CH1_SCL

I2C ADDRESS 0x6A

CLK_161.91P / CLK_161.91N

CLK_SD1_B_P/N, CLK_SD1_F_P/N

Boot select

SW1 SW DIP-S/SM

Rtn13 4x1K

Boot_Mode[0:3] 4C8

CFG_RCW_SRC1 … CFG_RCW_SRC5

Secure fuse processor voltage domain enable

U3015

EN_SFP_PROG → EN_SFP_PROG_3p3

R643 1K Assy = RUNTIME_PROG_SFP_CIR

MC74VHC1G125

SD interface with 1.8v/3.3v level shifter

U3014 NVT4857UK

SD_CLK_1v8 … SD_CMD_1v8 … SD_D0_1v8 … SD_D3_1v8 … SD_VSELECT

SD_CLK … SD_CMD … SD_D0 … SD_D3 … SD_CD

U90 SDHC #1 PORT

SDHC1_DAT0 … SDHC1_DAT3 / SDHC1_CLK / SDHC1_CD_b / SDHC1_DS / SDHC1_SCK / SDHC1_DAT4 … SDHC1_DAT7

SD_D0_1v8 … SD_D3_1v8 / SD_CMD_1v8 / SD_CLK_1v8 / SD_VSELECT / SD_CD

Connected to I2C2_SCL / I2C2_SDA

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eMMC

U90 SDHC #1 PORT

SDHC2_DAT0 … SDHC2_DAT7 / SDHC2_CMD / SDHC2_CLK / SDHC2_DS

U27 eMMC_153

DAT0 … DAT7 / CMD / CLK / RST_n / RCLK

LX2160 — R6.07B - 21 of 23

Reset button

U2 DTSM-3

Do not assemble C3. Assembling it confuses the bidirectional level shifter and can generate a reset loop.

Assy = UTAC_HEADER

1.8v / 3.3v level shifters

U1001 … U1007 NTSX2102GD

IRQ9_B, IRQ0_B → 10G_INT1, 10G_INT0

IRQ11_B, IRQ10_B → 10G_INT3, 10G_INT2

FAN_FULL_SPEED_1p8 → FAN_FULL_SPEED

PWM_PU

GPIO2_1p8 → GPIO2

THRM, SMB_ALERT#

PWRBTN_1p8 → PWRBTN#

SUS_S5_1p8 → SUS_S5#

EVT1_B, EVT0_B, EVT3_B, EVT2_B

JTAG

JTAG DEBUG HEADER

Cadi/Ramon CXITap or other JTAG-based tools.

U3014

PROC_TMS, PROC_TDI, PROC_TDO, PROC_TCK, JTAG_RST_B, MRst#, JTAG_VREF

20021121-00010C4LF

Assy = JTAG_HEADER

Boot SPI CS0/CS1 switch circuitry

BIOS_DS0#, BIOS_DS_OVERRIDE, BIOS_DS1_INVERTED

RESET_ACTIVE_HIGH

XSPI_A_CS0_B, XSPI_A_CS1_B → SPI_CS0#, SPI_1v8_CS1#

U17 SN74LVC1G373

U22 Dual SPDT

U18, U15 NC7SZ04

SPI controller, flash and level shifter

U26 SN74AVCA777APW

U90 DCTAL SPI

XSPI_A_CS0_B … XSPI_A_CS1_B, XSPI_A_D0 … XSPI_A_D7, XSPI_A_DQS, XSPI_A_SCK

SPI_CLK, SPI_MOSI, SPI_MISO, SPI_CS1#, SPI_1v8_CS1#

U8 MT35XU.....

Reset logic

SYS_RESET#, HRESET_B, PORESET_B, RESET_REQ_B

U3003 MC74VHC1GT08

U3005 MC74VHC1GT08

U39 PTTMD808QD1

U10067 74LVC1G125

SYSRST_OUT#, PORESET_B_3p3v

10nF delays the RESET# with 10ms

Boot select

SW DIP-S/SM

Rtn13 4x1K

Secure fuse processor voltage domain enable

U3015

EN_SFP_PROG → EN_SFP_PROG_3p3

R643 1K Assy = RUNTIME_PROG_SFP_CIR

MC74VHC1G125

SD interface with 1.8v/3.3v level shifter

U3014 NVT4857UK

SD_CLK_1v8 … SD_CMD_1v8 … SD_D0_1v8 … SD_D3_1v8 … SD_VSELECT

SD_CLK … SD_CMD … SD_D0 … SD_D3 … SD_CD

U90 SDHC #1 PORT

SDHC1_DAT0 … SDHC1_DAT3 / SDHC1_CLK / SDHC1_CD_b / SDHC1_DS / SDHC1_SCK / SDHC1_DAT4 … SDHC1_DAT7

SD_D0_1v8 … SD_D3_1v8 / SD_CMD_1v8 / SD_CLK_1v8 / SD_VSELECT / SD_CD

Connected to I2C2_SCL / I2C2_SDA

LX2160 — R6.07B - 15 of 23

eMMC

U90 SDHC #1 PORT

SDHC2_DAT0 … SDHC2_DAT7 / SDHC2_CMD / SDHC2_CLK / SDHC2_DS

U27 eMMC_153

DAT0 … DAT7 / CMD / CLK / RST_n / RCLK

LX2160 — R6.07B - 21 of 23

Reset button

U2 DTSM-3

Do not assemble C3. Assembling it confuses the bidirectional level shifter and can generate a reset loop.

Assy = UTAC_HEADER

1.8v / 3.3v level shifters

U1001 … U1007 NTSX2102GD

IRQ9_B, IRQ0_B → 10G_INT1, 10G_INT0

IRQ11_B, IRQ10_B → 10G_INT3, 10G_INT2

FAN_FULL_SPEED_1p8 → FAN_FULL_SPEED

PWM_PU

GPIO2_1p8 → GPIO2

THRM, SMB_ALERT#

PWRBTN_1p8 → PWRBTN#

SUS_S5_1p8 → SUS_S5#

EVT1_B, EVT0_B, EVT3_B, EVT2_B

JTAG

JTAG DEBUG HEADER

Cadi/Ramon CXITap or other JTAG-based tools.

U3014

PROC_TMS, PROC_TDI, PROC_TDO, PROC_TCK, JTAG_RST_B, MRst#, JTAG_VREF

20021121-00010C4LF

Assy = JTAG_HEADER

Boot SPI CS0/CS1 switch circuitry

BIOS_DS0#, BIOS_DS_OVERRIDE, BIOS_DS1_INVERTED

RESET_ACTIVE_HIGH

XSPI_A_CS0_B, XSPI_A_CS1_B → SPI_CS0#, SPI_1v8_CS1#

U17 SN74LVC1G373

U22 Dual SPDT

U18, U15 NC7SZ04

SPI controller, flash and level shifter

U26 SN74AVCA777APW

U90 DCTAL SPI

XSPI_A_CS0_B … XSPI_A_CS1_B, XSPI_A_D0 … XSPI_A_D7, XSPI_A_DQS, XSPI_A_SCK

SPI_CLK, SPI_MOSI, SPI_MISO, SPI_CS1#, SPI_1v8_CS1#

U8 MT35XU.....

Reset logic

SYS_RESET#, HRESET_B, PORESET_B, RESET_REQ_B

U3003 MC74VHC1GT08

U3005 MC74VHC1GT08

U39 PTTMD808QD1

U10067 74LVC1G125

SYSRST_OUT#, PORESET_B_3p3v

10nF delays the RESET# with 10ms

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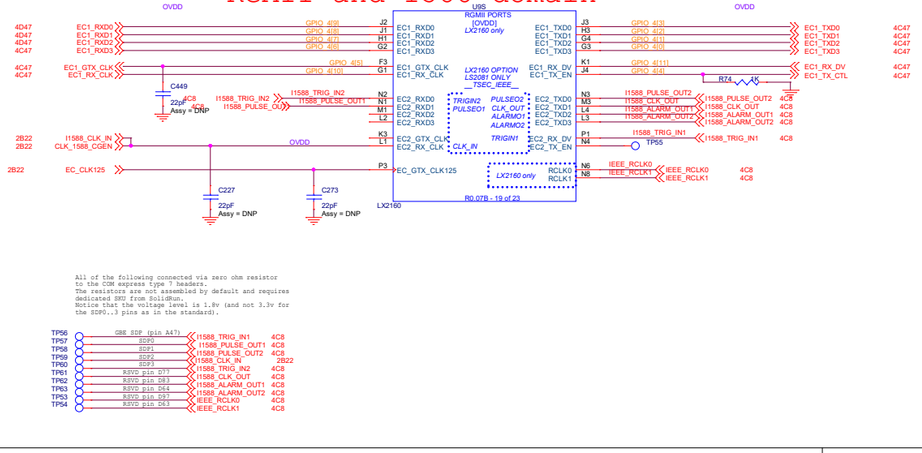
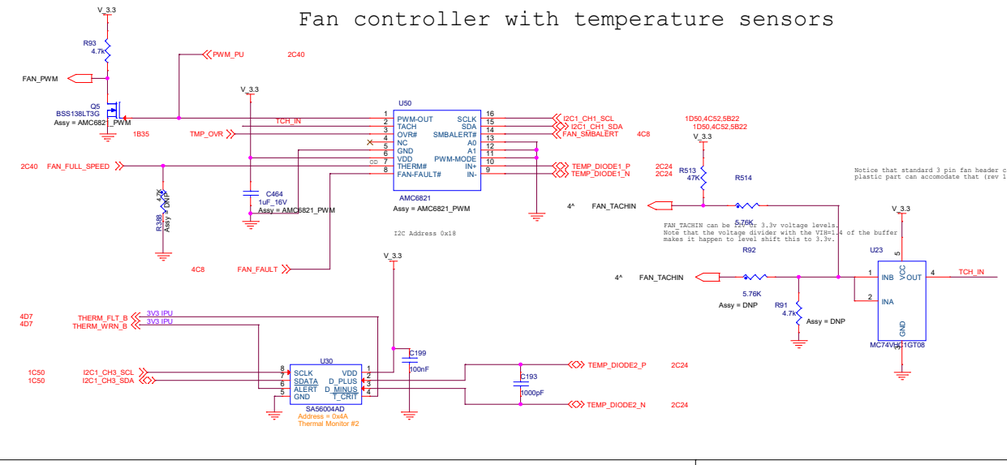
SolidRun | Size: E | File: LX2160A-CEx7 Simplified Schematics | Rev: 2.1 | Date: Sunday, June 18, 2023 | Sheet: 1 of 3

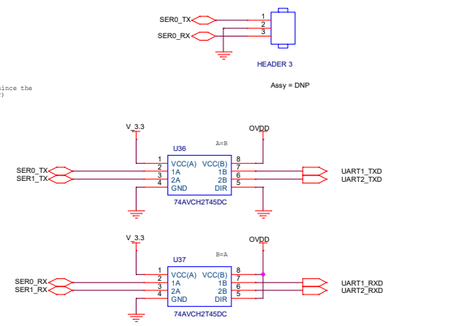
RGMII and 1588 domain



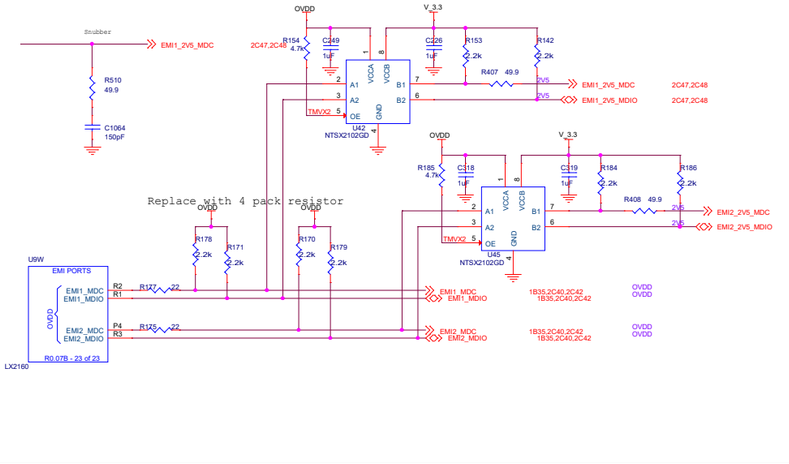
Fan controller with temperature sensors



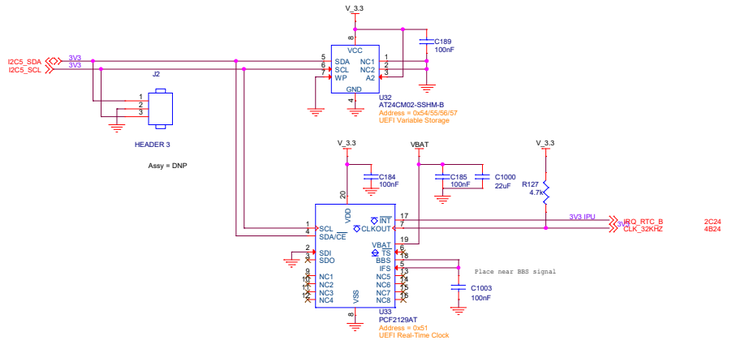
Serial UART 0 and 1



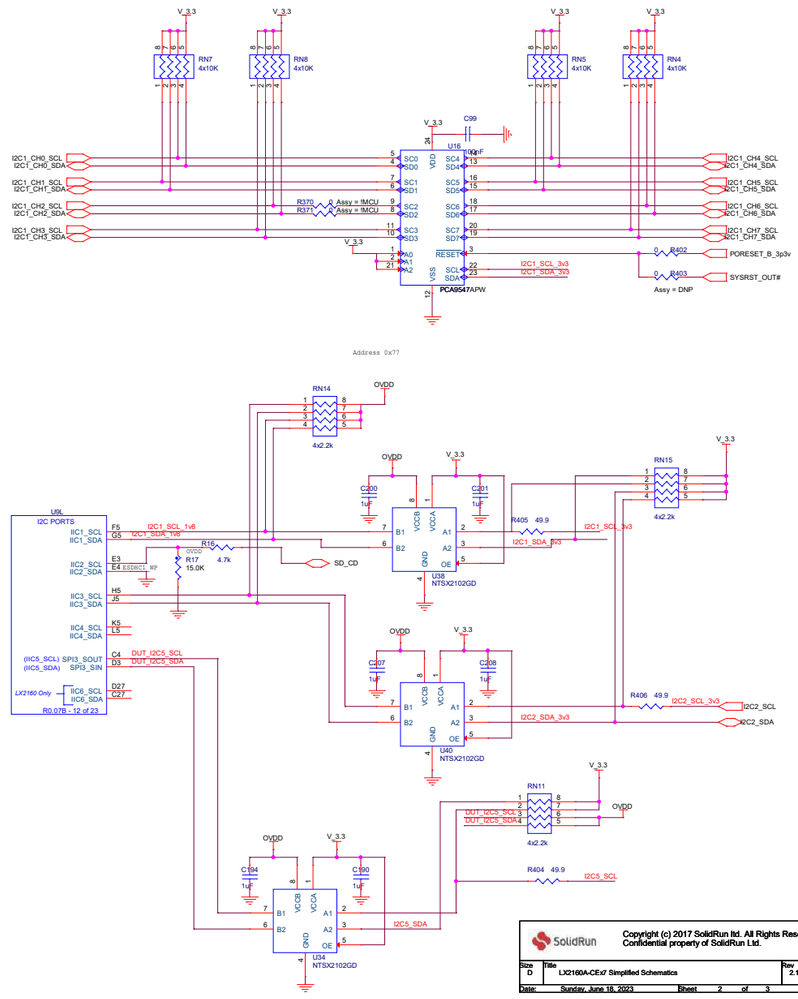
Dual MDC/MDIO with level shifters



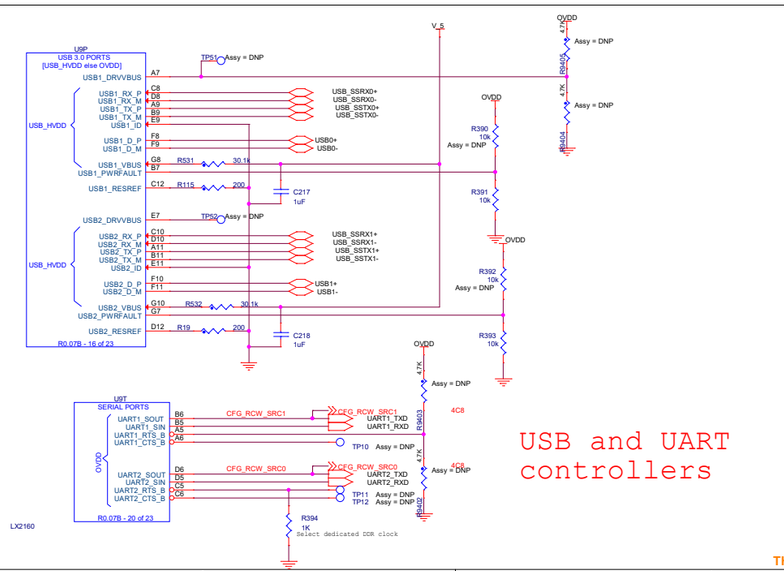
2Mb I2C EEPROM and RTC controller



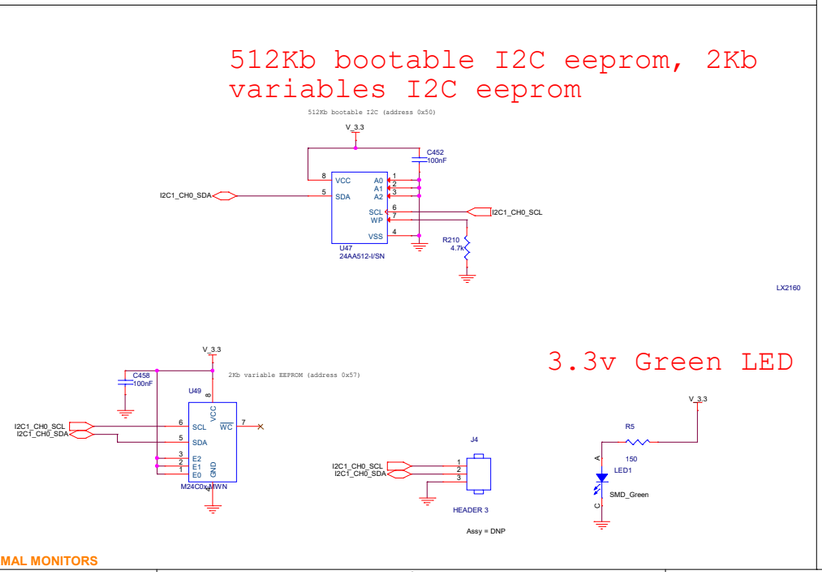
I2C Controllers and MUX



USB and UART controllers



512Kb bootable I2C eeprom, 2Kb variables I2C eeprom



THERMAL MONITORS

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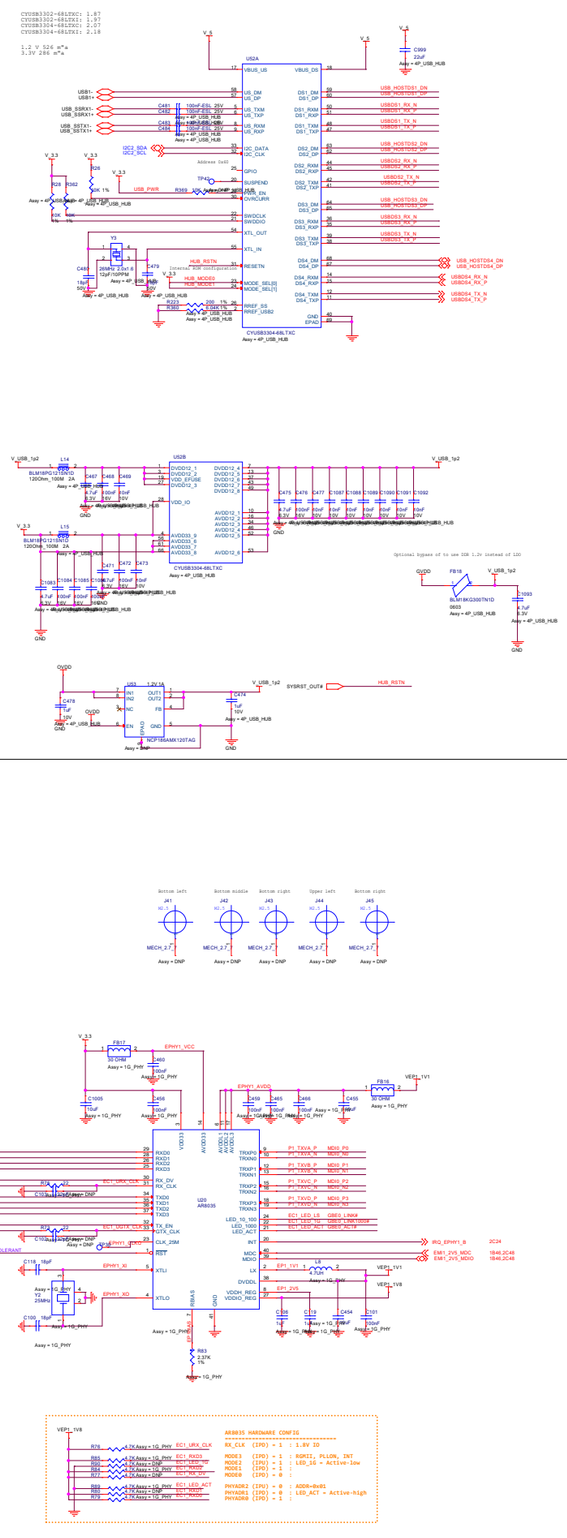
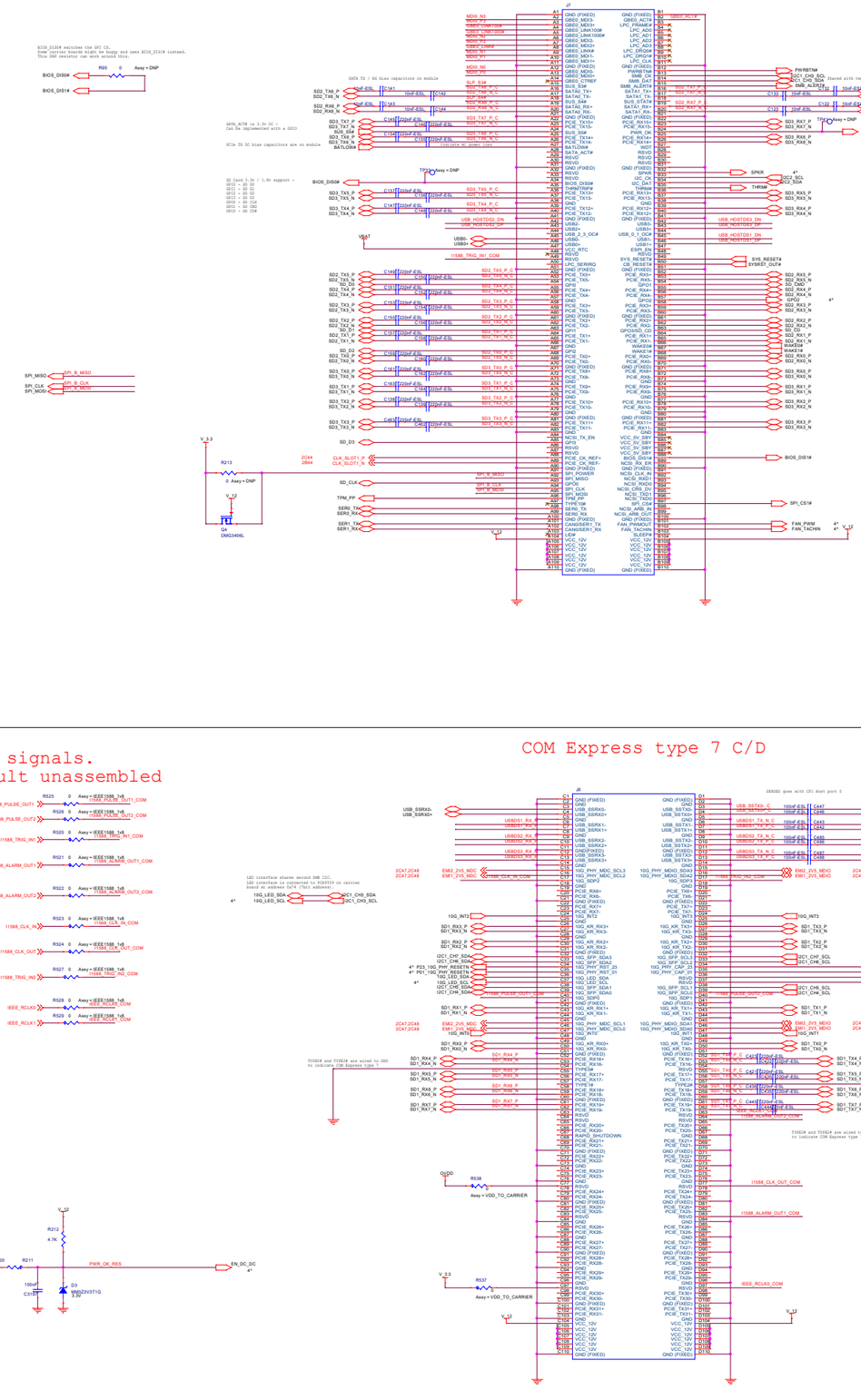
Size	Title	Rev
D	LX2160A-CEx7 Simplified Schematics	2.1
Date: Sunday, June 18, 2023	Sheet 2 of 3	

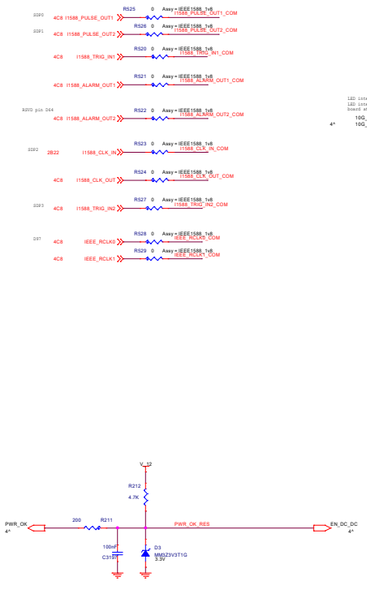
1Gbps Ethernet copper



COM Express type 7 A/B



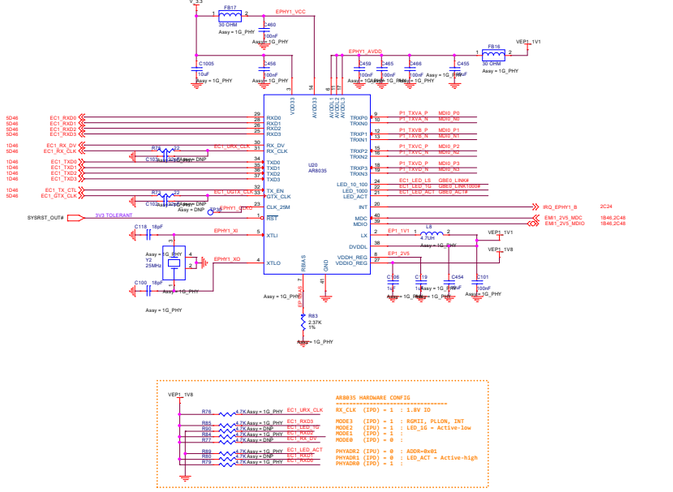
1588 signals. Default unassembled



COM Express type 7 C/D

Mechanical

Ethernet PHY


EPHY1_VCC
EPHY1_AVDD
VEP1_1V1
VEP1_1V8
FB17
FB16
C460 100nF
C1005 10uF
C456 100nF
C455 100nF
C458 100nF
C459 100nF
C466 100nF
C465 100nF
C419 100nF
Assy = 1G_PHY
U29
AR8035
AVDD33
AVDD11
AVDD12
EC1_RXD0
EC1_RXD1
EC1_RXD2
EC1_RXD3
EC1_RX_DV
EC1_RX_CLK
EC1_TXD0
EC1_TXD1
EC1_TXD2
EC1_TXD3
EC1_TX_CTL
EC1_GTX_CLK
EC1_GTX_CLK_1
R24 22
R25 22
SYSRST_OUT#
3V3_TOLERANT
EPHY1_25M
EPHY1_XI
EPHY1_XO
Y3 25MHz
C116 18pF
C100 18pF
C108 1uF
C113 1uF
C454 100nF
C101 100nF
R84 2.37K 1%
R83 2.37K 1%
P1_TXVA_P
P1_TXVA_N
P1_TXVB_P
P1_TXVB_N
P1_TXVC_P
P1_TXVC_N
P1_TXVD_P
P1_TXVD_N
MDI0_P0
MDI0_N0
MDI0_P1
MDI0_N1
MDI0_P2
MDI0_N2
MDI0_P3
MDI0_N3
LED_1G_1G
LED_100_ACT
LED_LG
GBE1_LINK1000#
LED_100_ACT
GBE1_ACT#
MDC
MDIO
IRQ_EPHY1_B
2C24
EM1_3V3_MDC
EM1_3V3_MDIO
1B46,2C48
EP1_1V1
EP1_2V5
VDDH_REG
VDDIO_REG
VEP1_1V8
VEP1_1V3
L5 4.7uH
C1092 10uF
C1093 4.7uF
C1094 10uF
C1095 10uF
C1096 10uF
C1097 10uF
C1098 10uF
C1099 10uF
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C1109 10uF
C1110 10uF
C1111 10uF
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C1113 10uF