

ClearFog LX2162A

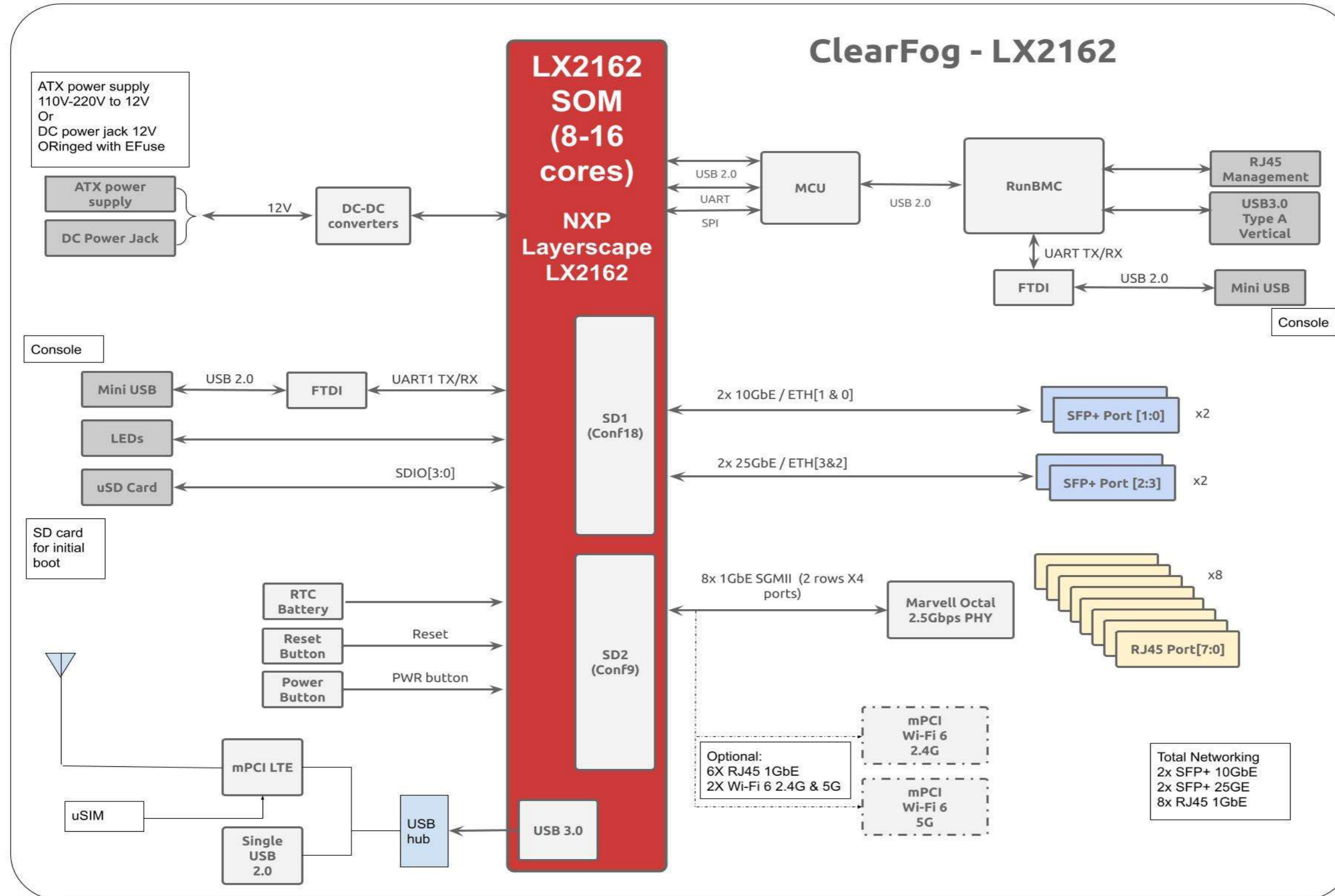
SolidRun Ltd.

Revision History

Rev#	Date	Owner	Description
1.0	Feb 2022	IlanB	First Release

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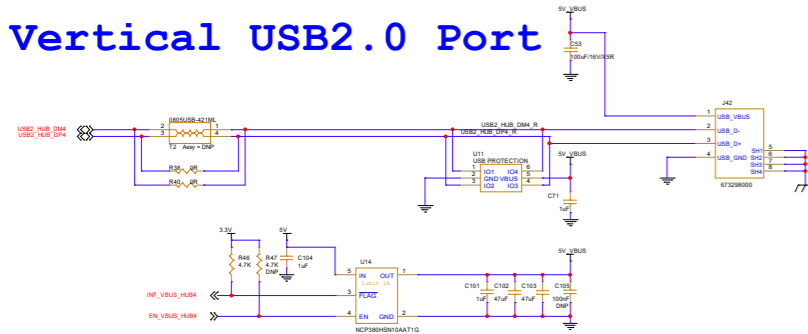
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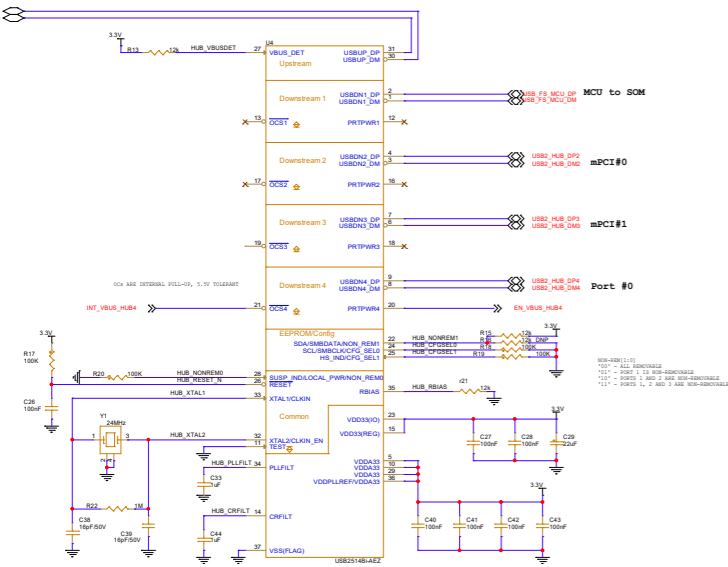
SOM & SFP

LX2162-SOM Interface

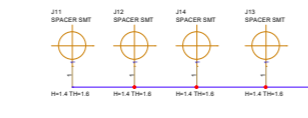
Vertical USB2.0 Port



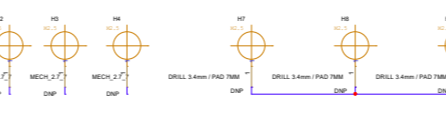
USB2.0 HUB



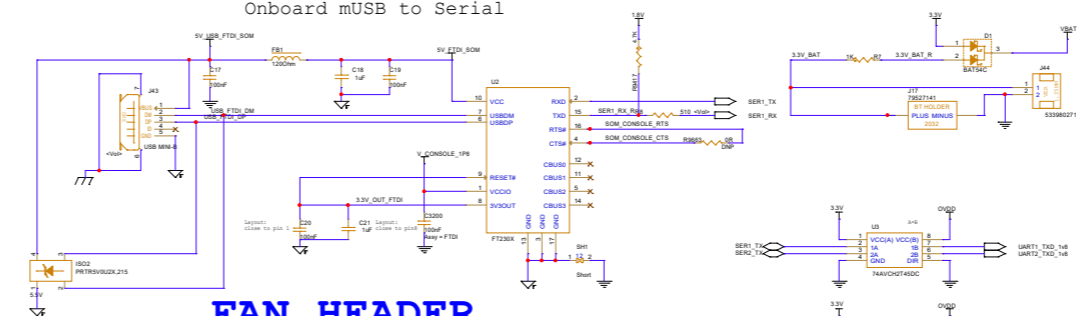
SOM Spacers



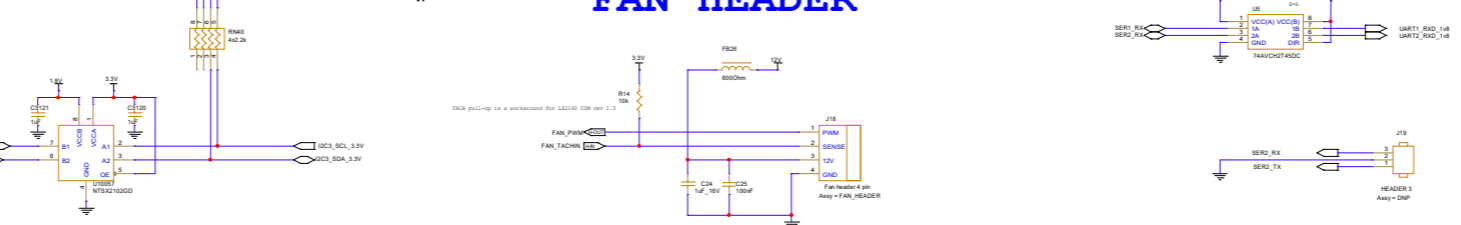
Mechanical Holes



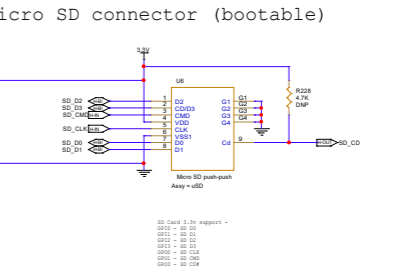
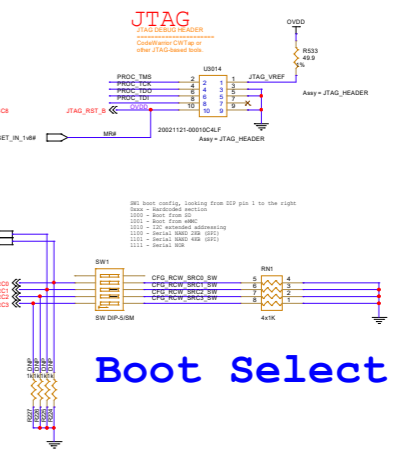
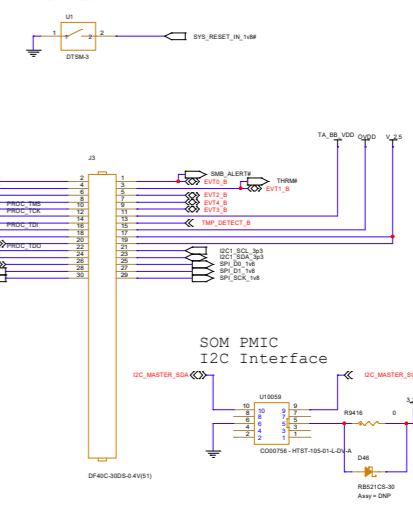
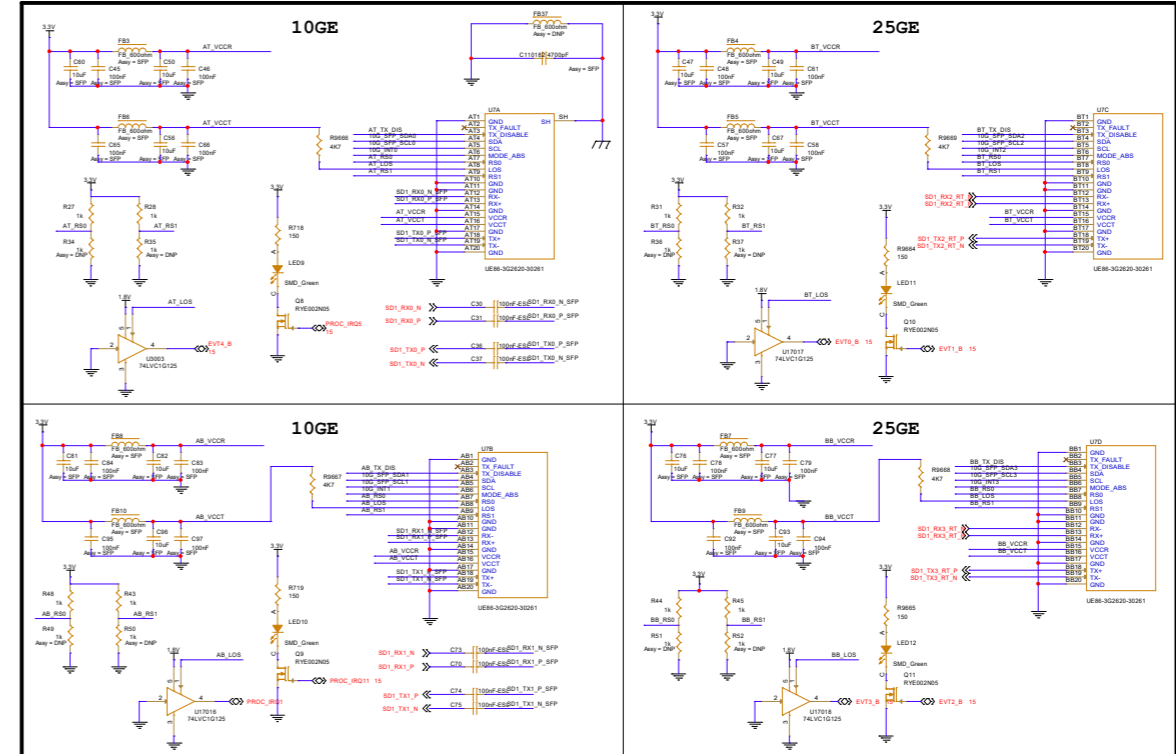
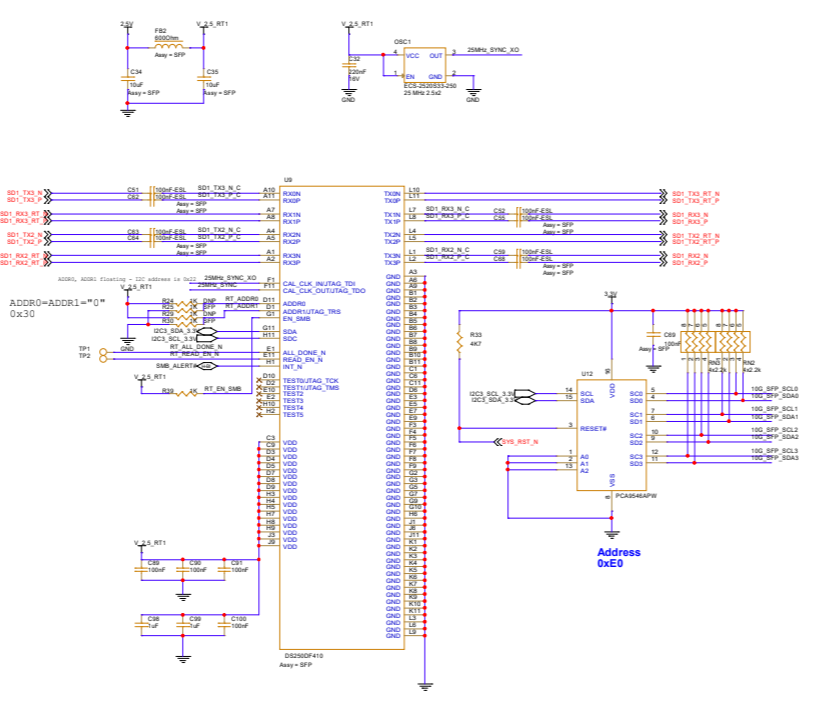
Onboard mUSB to Serial



FAN HEADER



SFPs

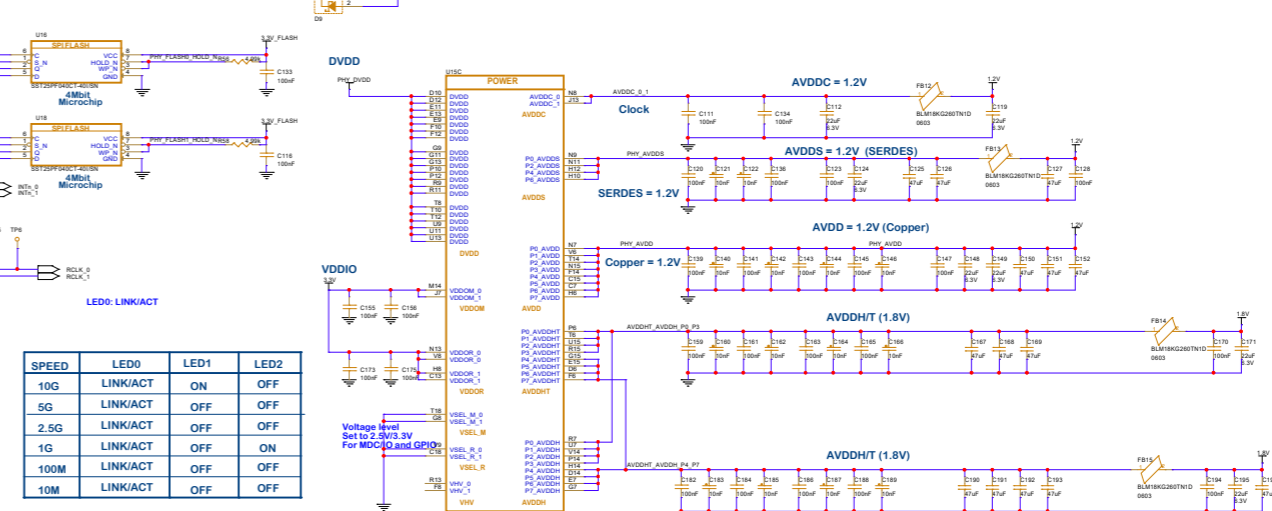
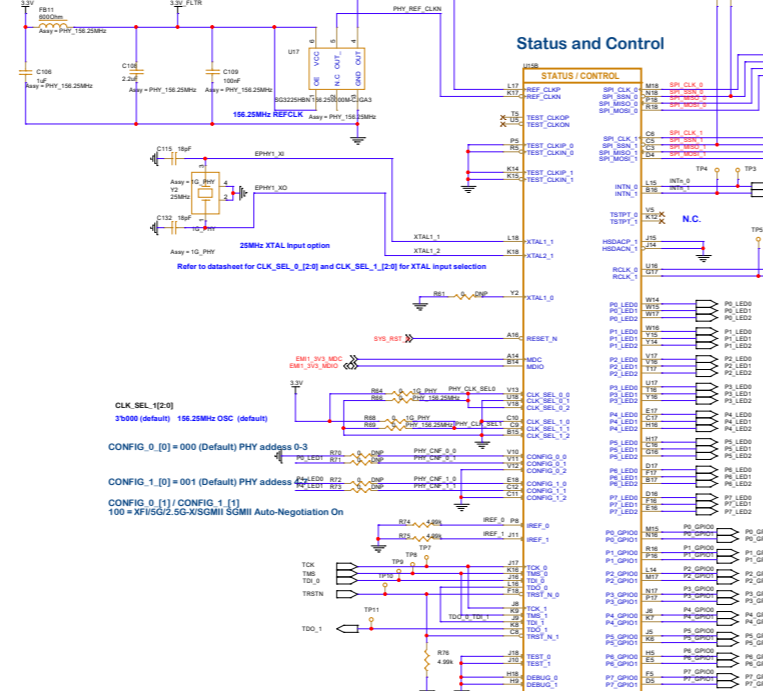
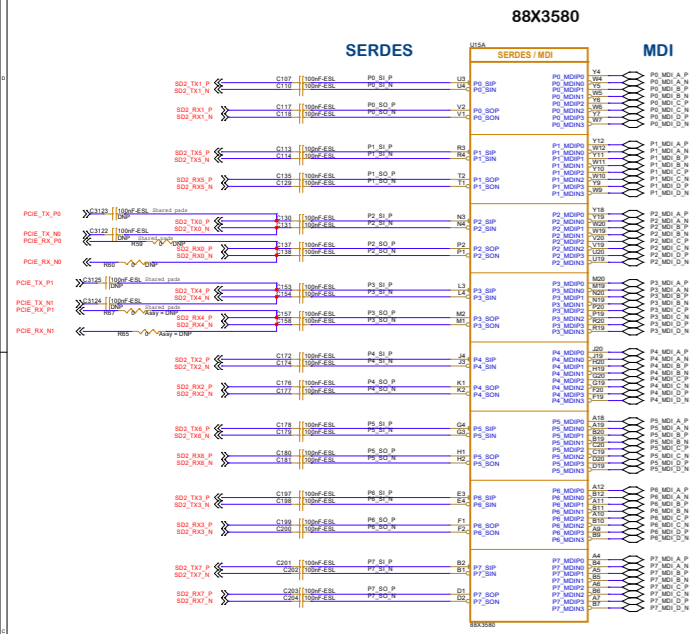


History Revision	
00	First Release

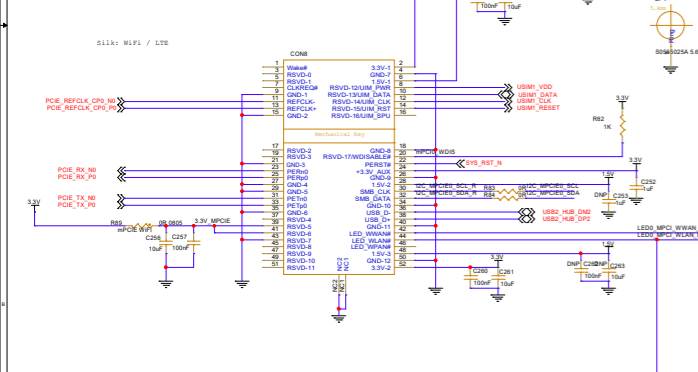
RJ45 & PHY

Power Consumption PHY (per port):
 SGMII - 0.8V -> 240mA
 1.2V -> 200mA
 1.8V -> 435mA
 Total -> 1.215W per PORT X8 = 9.72W

Power Consumption PHY (per port):
 2.5G - 0.8V -> 465mA
 1.2V -> 225mA
 1.8V -> 474mA
 Total -> 1.495W per PORT X8 = 11.96W

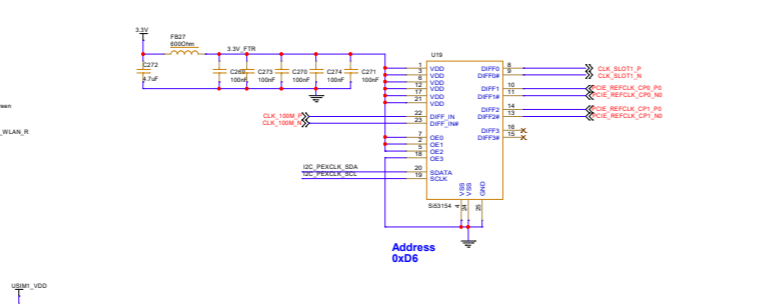


PCIe X1 Gen3 802.11ac wave2 or LTE 4G mPCIe #0

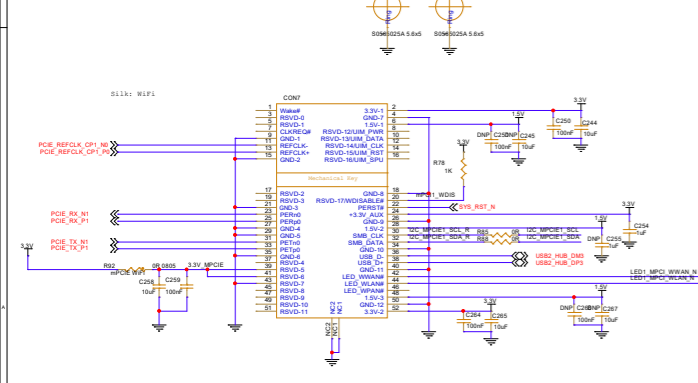


MACTYPE[2:0]: 31.F001.2.0 <= cfg_MACTYPE[2:0];
 000 = SXGMII
 001 = DXGMII
 010 = CXGMII
 011 = OXGMII
 100 = XF15G/2.5G-X/SGMII SGMII Auto-Negotiation On
 101 = 10GKR/5.0GKR/2.5GKR/1000BASE-X CL73
 110 = Rate Matching Mode, AMD Mode
 111 = Reserved

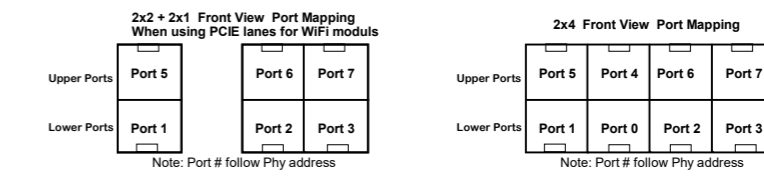
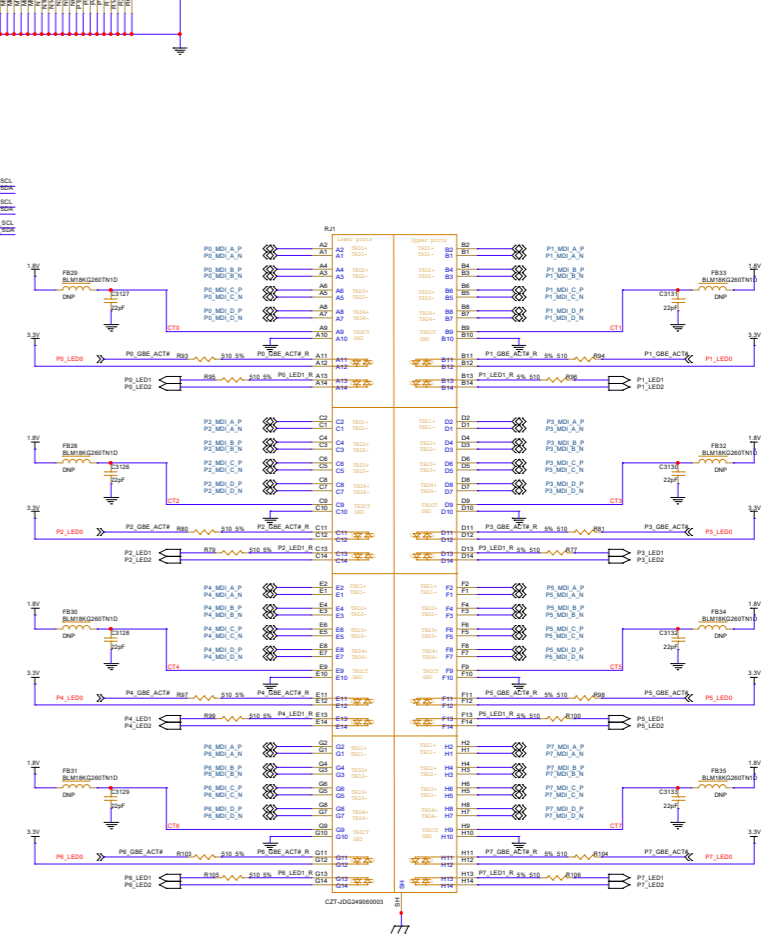
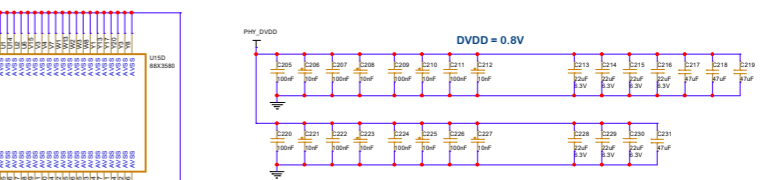
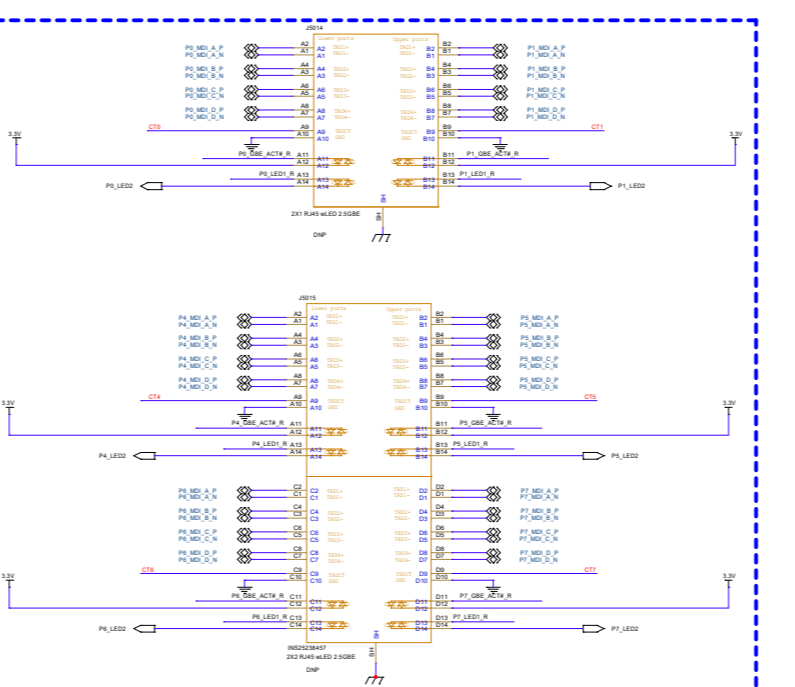
PCIe Clock



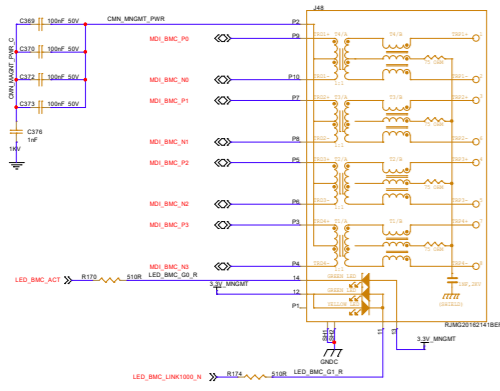
PCIe X1 Gen3 802.11ac wave2 mPCIe #1



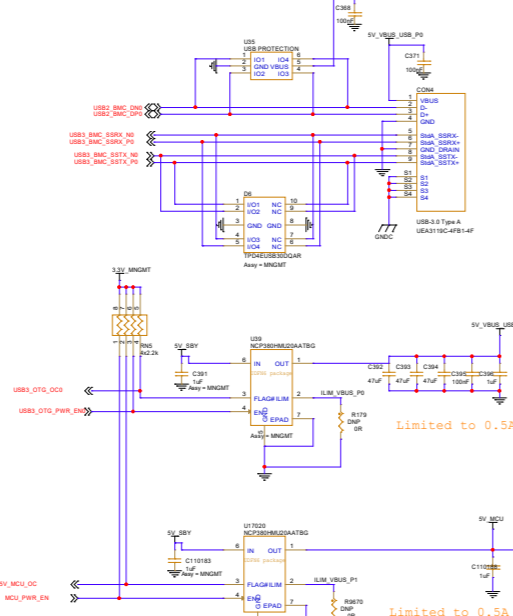
Assemble only when using PCIE lane for WiFi



RJ45

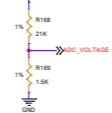


Vertical USB3.0

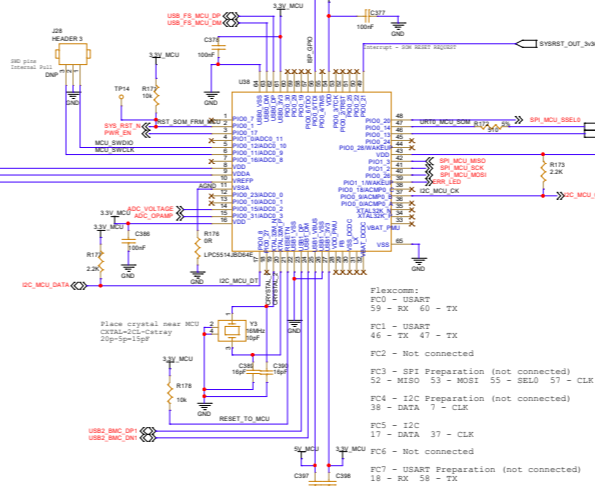


RUNBMC

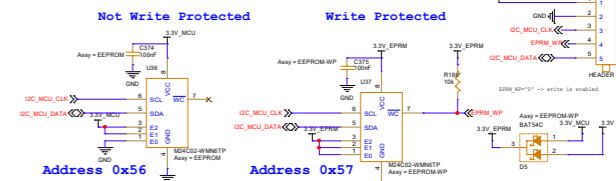
Voltage Measurement



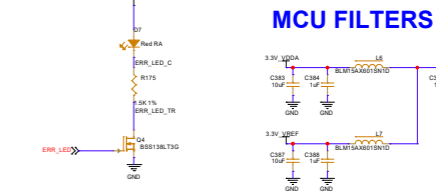
MCU



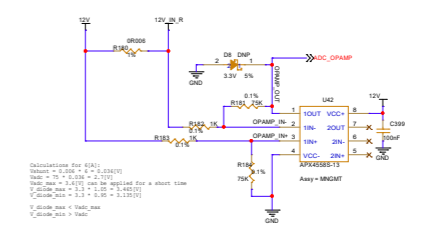
2Kbit EEPROMS-MCU



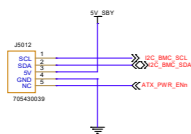
RED LED



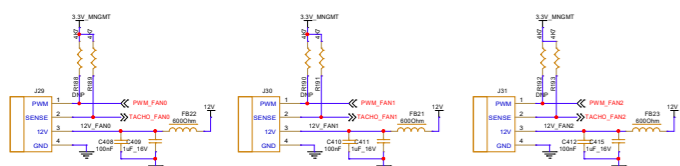
Power Measurement



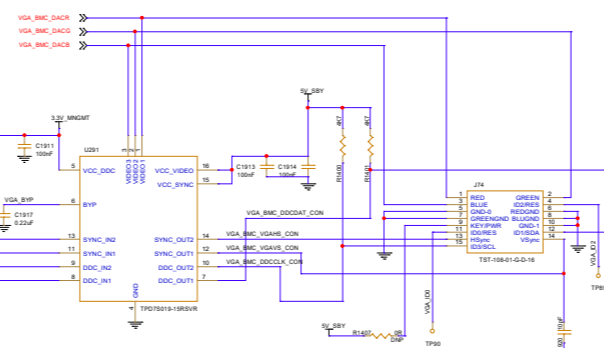
ATX PWR Board MNGMT



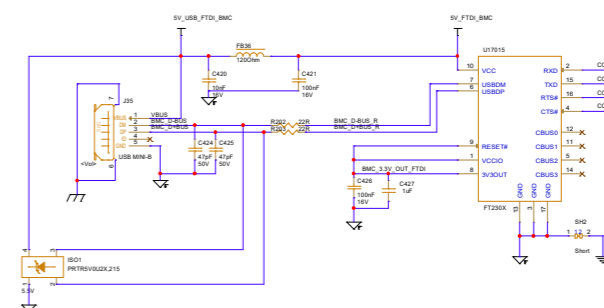
FAN Connectors



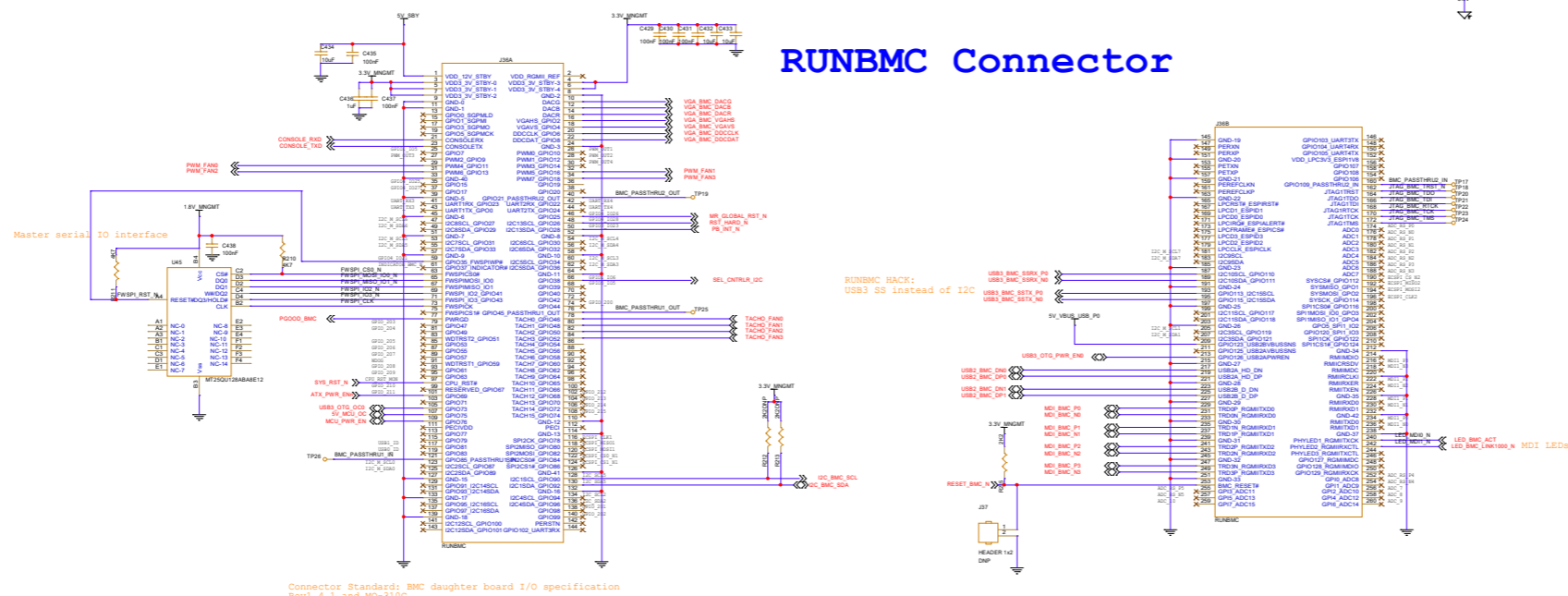
VGA



Console



RUNBMC Connector



RUNBMC HACK: USB3 SS instead of I2C

Connector Standard: BMC daughter board I/O specification Rev1.4.1 and MD-310C