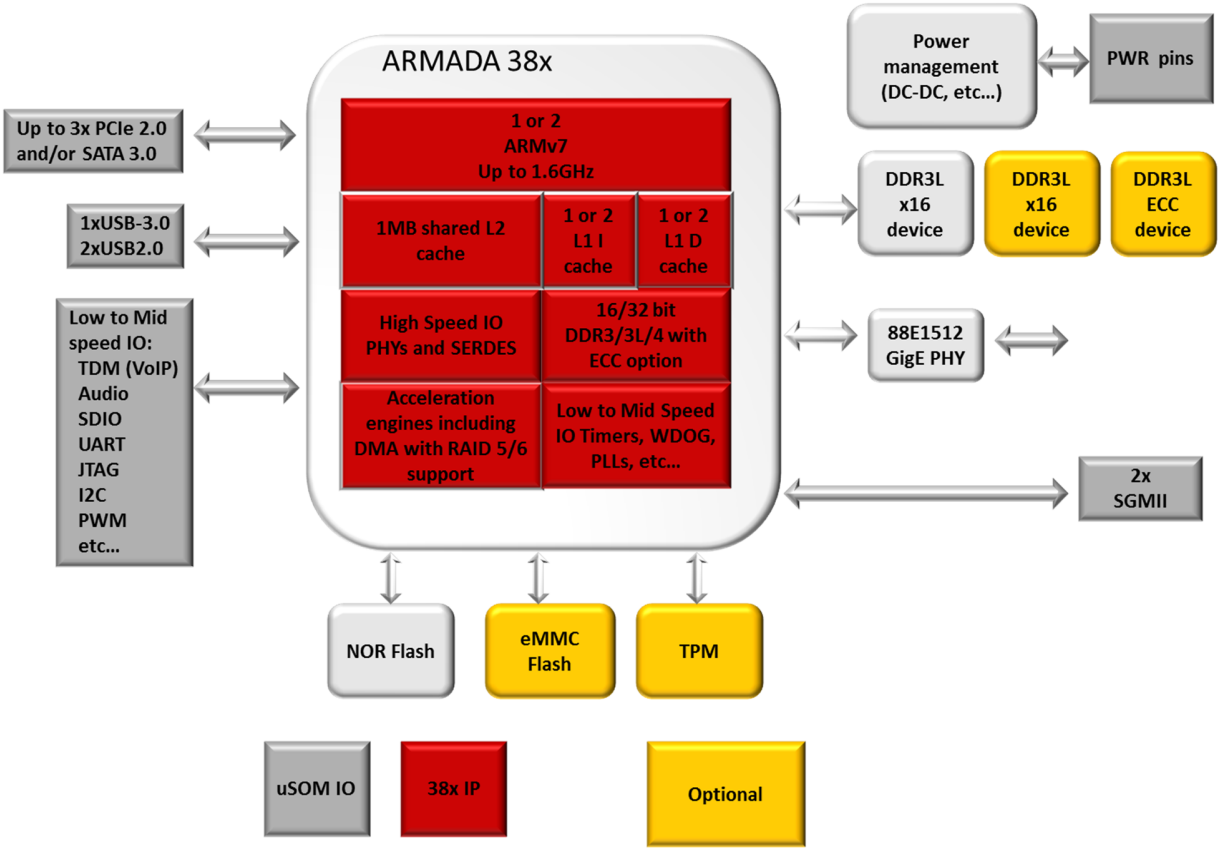
A38x-uSoM Integration Guide

Date	Owner	Revision	Notes
October 11th 2015	Kossay Omary	0.1	Preliminary release

A38x MicroSoM Block Diagram



Connecting to the A38x MicroSoM:

The A38x-uSoM has two Board-to-Board connectors used to connect to the carrier board. The MicroSoM uses an 80 pin header from Hirose (part number "**DF40C-80DP-0.4V(51)**"). The carrier board must use a mating Hirose Receptacle such as the "**DF40C-80DS-0.4V(51)**" (producing 1.5mm mating height). Other Receptacles can be used to produce different mating heights up to 4.0mm.

The Board-to-Board pins are used for a variety of functionalities and purposes. The following sections describe those in detail.

Power and Power Management

The A38x-uSoM has one global ground domain, four power input domains and one power output domain.

Name	Description	Voltage	Power	Notes / Instructions
GND	Global Ground Net	N/A	N/A	Connect to carrier ground plane.
B2B_V_MAIN	Main voltage domain	3.3v-5.0v	7.5W[1]	Connect to 5.0V DC-DC output or to 3.3V DC-DC output (or any value between).
B2B_V_3V3	Low speed I/O domain	3.3V	0.75W	Connect to 3.3V DC-DC output.
B2B_V_RTC		3.0V – 3.3V	~0w	Recommend to use two diodes to connect to backup battery and to B2B_V_3V3
B2B_V_1V8_VHV		1.8V	~0w	Connect to B2B_V_1V8 to enable programming internal fuses. Otherwise keep floating.

Notes:

1- Power consumption of 7.5W on B2B_V_MAIN domain assuming all devices are assembled and all functions are operating at full utilization.

The A38x-uSoM has one B2B_V_1V8 output power domain which is used to power the High Speed SERDES PHYs as well as the GigE PHY. In addition to those loads, the B2B_1V8 source can provide additional 0.5A to loads on carrier board.

In addition to the power domain signals, there are other signals which are used for power management and power-up/down sequencing:

Name	Pullup/down	Description	Level	Notes / Instructions
B2B_1V8_1V35_EN	None	Enable signal of MicroSoM I/O DC-DC.		Do not float. Pullup to B2B_V_MAIN
B2B_1V8_PWR_EN	PU (100 kΩ) to B2B_V_3V3	Advance power management		Do not connect to this signal.
B2B_MV_VSDRAM_PWR_EN	PU (100 kΩ) to B2B_V_3V3	Advance power management		Do not connect to this signal.
B2B_OD_3V3_PG	PU (4.7 kΩ) to	Carrier based DC-		Drive low until all

	B2B_V_MAIN	DC units feeding MicroSoM are stable. Triggers CPU/Core DC-DC to start operating.		power inputs to MicroSoM are stable. Also Drive low to disable CPU/Core power domain.
B2B_V_CPU_CORE_PG	OD	Indicates that CPU/Core power domain is up. This also means all other domains on the MicroSoM are up as well.		If this signal needs to be sampled then add a 4.7 kΩ pullup resistor.

Power up sequence

The A38x-uSoM requires that all power inputs are stable before allowing B2B_OD_3V3_PG to go high. Use DC-DC devices with power-good indication and drive B2B_OD_3V3_PG low as long as the power-good indications MicroSoM voltages are driven low.

System Reset

Name	Pullup/down	Description	Notes / Instructions
B2B_MRN	PU (100 kΩ) to B2B_V_3V3	Manual Reset input. B2B_SYSRST_OUTN is driven low for as long as B2B_MRn is driven low plus additional 100mS after B2B_MRn is de-asserted.	Connect to system push button reset or other system reset triggers. Make sure it is pulled high when not active. See ClearFog Pro reference design schematics.
B2B_SYSRST_OUTN	PU (4.7 kΩ) to B2B_V_3V3	Active low reset output asserted when B2B_MRn is asserted, plus additional 100mS. Power on reset circuit will trigger B2B_SYSRST_OUTN as well.	This signal should be used to reset any device in the system that is intended to be reset by the B2B_MRn reset event.
B2B_SYSRST_INN	None	Armada 38x input reset signal.	Short to B2B_SYSRST_OUTN to trigger Armada 38x reset on B2B_MRn reset trigger event.

Multi-Purpose Pins (MPP)

The Armada 38x has 60 Multi Purpose Pins. Each of those can be programmed to be a GPIO, Interrupt input or have a specialized function. Appendix-A for details.

Out of the 60 pins 12 signals are used as RGMII0 on the MicroSoM to connect to the GigE PHY and are not connected to the Board-to-Board (except MPP[7:9] who are exposed to the Board-to-Board for the mere purpose of sampling at reset the boot select field.). The remainder pins can be used as GPIO, Interrupt input, UART, I2C, SPI, SDIO, PWM and more. Check spreadsheet in Appendix-A for more details.

Please notice that, if assembled, the onboard SPI ROM is connected to B2B_MPP pins 56:59. Also, if assembled the eMMC device on the MicroSoM is connected to B2B_MPP pins 21, 28 and 37:40. If assembled those signals are terminated at the eMMC device and are not exposed to the Board-to-Board connector. Otherwise they are connected to the Board-to-Board in order to be potentially used on the carrier board.

For proper operation of the system, special attention is required for the following.

Board-to-Board signal	**Domain**	**Default Pull-up/down**	**Special function / instructions.**
B2B_UA0_RXD (MPP0)	V_3V3	PD	
B2B_UA0_TXD (MPP1)	V_3V3	PD (510 Ω)	Reserved. Pull down or float during reset.
B2B_I2C0_SCK (MPP2)	V_3V3	PU (4.7 kΩ)	
B2B_I2C0_SDA (MPP3)	V_3V3	PU (4.7 kΩ)	
B2B_GE_MDC (MPP4)	V_1V8	PD (510 Ω)	CPU0 Endianess. Do not modify default pull-up/down during reset.
B2B_BOOT_SEL_0 (MPP7)	V_1V8	PD	Boot Device Mode[0]. Pull-up/down based on desired boot device.
B2B_BOOT_SEL_1 (MPP8)	V_1V8	PU	Boot Device Mode[1]]. Pull-up/down based on desired boot device.
B2B_BOOT_SEL_2 (MPP9)	V_1V8	PU	Boot Device Mode[2]]. Pull-up/down based on desired boot device.
B2B_MPP22	V_3V3	PD	CPU0 Thumb Exception Init. Do not modify default pull-up/down during reset.
B2B_MPP23	V_3V3	PU	PCI0 Express Clock Configuration
B2B_MPP28	V_3V3	PD	I2C Serial ROM Initialization
B2B_MPP29	V_3V3	PD	Core Clock Frequency Select
B2B_MPP30	V_3V3	PD	CPU Subsystem Clock Frequency Options[1]
B2B_MPP31	V_3V3	PU	CPU Subsystem Clock Frequency Options[2]
B2B_MPP32	V_3V3	PD	CPU0 NMFI Enable. Do not modify default pull-up/down during reset.
B2B_MPP33	V_3V3	PD	CPU Subsystem Clock Frequency Options[0]
B2B_MPP34	V_3V3	PU	CPU Subsystem Clock Frequency Options[3]
B2B_MPP35	V_3V3	PD	CPU Subsystem Clock Frequency Options[4]
B2B_MPP36	V_3V3	PU	Reserved. Do not pull up or down during reset.
B2B_MPP38	V_3V3	PU	Revision ID - Do not pull up or down during reset.
B2B_MPP39	V_3V3	PU	Revision ID - Do not pull up or down during reset.
B2B_MPP40	V_3V3	PU	Revision ID - Do not pull up or down during reset.
B2B_MPP42	V_3V3	PU	Boot Device Mode[4]]. Pull-up/down based on desired boot device.

B2B_MPP44	V_3V3	PU	Reserved. Do not pull up or down during reset.
B2B_MPP47	V_3V3	PD	Reserved. Do not pull up or down during reset.
B2B_MPP51	V_3V3	PD	SSCG Disable. Do not modify default pull-up/down during reset.
B2B_MPP56	V_3V3	PU	Boot Device Mode[5]]. Pull-up/down based on desired boot device.
B2B_MPP57	V_3V3	PD	Boot Device Mode[3]]. Pull-up/down based on desired boot device.

High Speed SERDES

A38x-uSoM modules based on Marvell 88F6810 SoC (single core) have five High Speed SERDES lanes and modules based on Marvell 88F6820 and 88F6828 SoC have 6 lanes. The high speed lanes can be configured to support PCIe gen 2, SATA gen 3 (6Gbps), SGMII (up to 2.5Gbps), QSGMII or USB-3.0.

Table 39: 88F6810 SERDES Lane Selection Options

Interface	SRD 0 (Lane 0)	SRD 1 (Lane 1)	SRD 2 (Lane 2)	SRD 3 (Lane 3)	SRD4 (Lane 4)	SRD 5 (Lane 5)
PCIe	PCIe 0 RC/EP	PCIe 0 RC/EP	-	PCIe 3 RC	-	PCIe 2 RC
PCIe x4 / PCIe	-	-	-	-	-	-
SATA	SATA 0	SATA 0	SATA 1	-	-	-
SGMII	SGMII 0	SGMII 0 or SGMII 1	SGMII 1	-	-	-
USB 3 Host	-	USB3 0 (H)	-	USB3 1 (H)	-	USB3 1 (H)
USB 3 Device	-	-	-	USB3 0 (D)	-	USB3 0 (D)
QSGMII	-	-	-	-	-	-

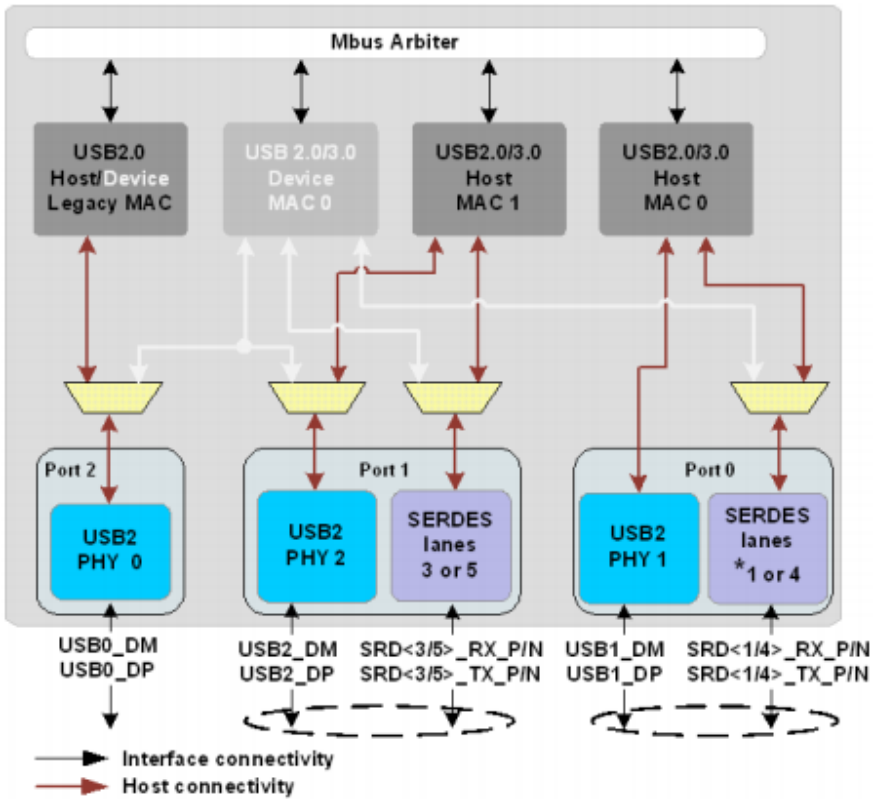
Table 41: 88F6828 SERDES Lane Selection Options

Interface	SRD 0 (Lane 0)	SRD 1 (Lane 1)	SRD 2 (Lane 2)	SRD 3 (Lane 3)	SRD 4 (Lane 4)	SRD 5 (Lane 5)
PCIe	PCIe 0 RC/EP	PCIe 0 RC/EP	PCIe 1 RC	PCIe 3 RC	PCIe 1 RC	PCIe 2 RC
PCIe x4 / PCIe	PCIe 0-L0 RC/EP	PCIe 0-L1 RC/EP	PCIe 0-L2 RC/EP	PCIe 0-L3 RC/EP	PCIe 2 RC	-
SATA	SATA 0	SATA 0	SATA 1	SATA 3	SATA 2	SATA 2
SGMII	SGMII 0	SGMII 0 or SGMII 1	SGMII 1	SGMII 2	SGMII 1	SGMII 2
USB3 Host	-	USB3 0 (H)	-	USB3 1 (H)	USB3 0 (H)	USB3 1 (H)
USB3 Device	-	-	-	USB3 0 (D)	USB3 0 (D)	USB3 0 (D)
QSGMII	-	QSGMII	-	-	-	-

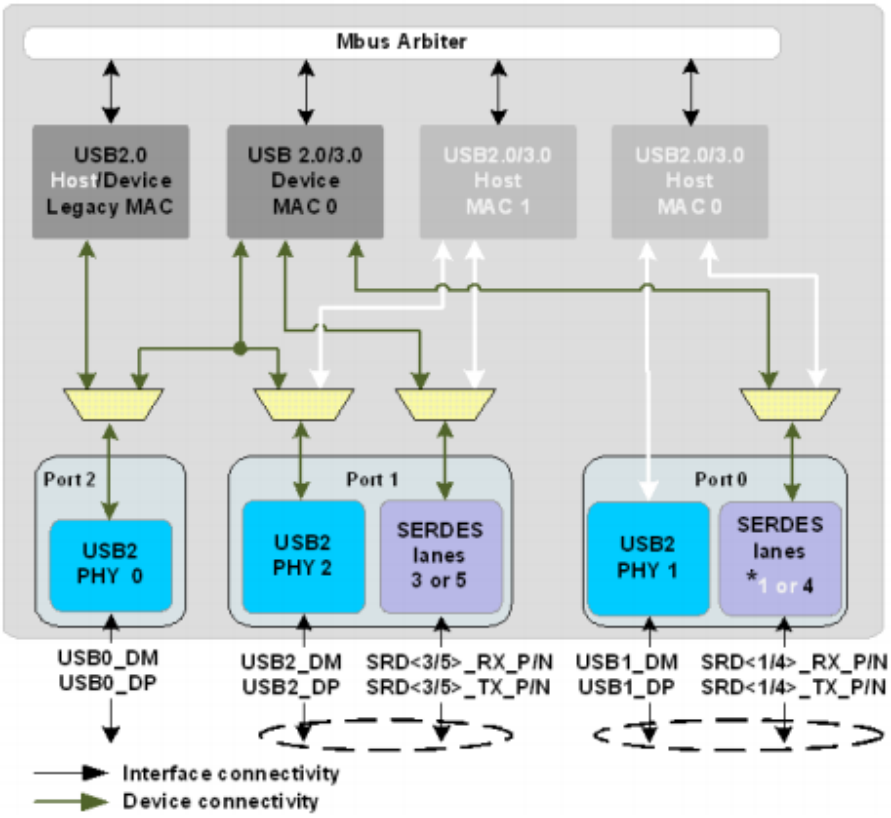
High Speed SERDES layout guidelines

TBD.

USB Host connectivity



USB Device connectivity



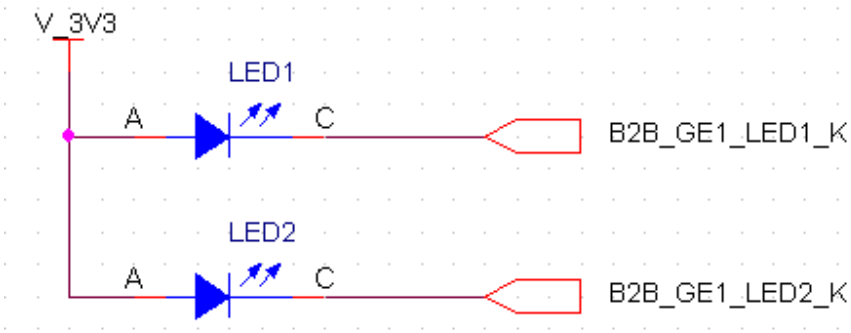
Integrated GigE PHY

A GigE PHY (Marvell 88E1512) is integrated into the A38x-uSoM and is connected to MAC0 via the SoC's RGMII-0 interface. The following PHY interfaces are exposed to the Board-to-Board connector

Interface	Domain	**Pullup/down**	**Special function / instructions.**
MDIO	N/A	N/A	Four Differential pairs carrying network traffic.
B2B_PHY1_INTN	B2B_V_1V8	PU (10 kΩ)	Interrupt output of GigE PHY
B2B_PHY1_RSTN	B2B_V_1V8	PU (4.7 kΩ)	Reset input of the GigE PHY.
B2B_GE1_LED1_K	B2B_V_1V8	510 Ω series resistor	Drive low on link. Blink on activity.[1]
B2B_GE1_LED2_K	B2B_V_1V8	510 Ω series resistor	Drive low on 1000Mbps link[1]

NOTE-1: Based on default PHY device driver programming of PHY configuration registers.

Following is one way of connecting the B2B_GE1_LEDx_K signals to the actual LED devices. Notice that the LED devices must have a high enough V_f (Forward voltage) to ensure no light is emitted when the B2B_GE1_LEDx_K signals are high (approximately 1.8v).



JTAG

TBD

If unused, JTAG signals B2B_JT_x and B2B_CDRn can be left floating.

Miscellaneous

Boot Device setting

Setting	Details
0X0	BootROM Enabled, Boot from NOR:8 bits width,DEV_Wen and DEV_Oen are not muxed with DEV_A(16:15), using MPP multiplexing option of NOR 8 bits
0X1	BootROM Enabled, Boot from NOR:8 bits width,DEV_Wen and DEV_Oen are muxed with DEV_A(16:15), using MPP multiplexing option of NOR 8 bits
0X4	BootROM Enabled, Boot from NOR:16 bits width,DEV_Wen and DEV_Oen are not muxed with DEV_A(16:15), using MPP multiplexing option of NOR 16 bits
0X5	BootROM Enabled, Boot from NOR:16 bits width,DEV_Wen and DEV_Oen are muxed with DEV_A(16:15), using MPP multiplexing option of NOR 16 bits
0X6	Reserved
0X7	Reserved
0X8	BootROM Enabled, Boot from NAND:8 bits width,with page size of 512B, 3 Address cycles support per page, using MPP multiplexing option of NAND 8 bits
0X9	BootROM Enabled, Boot from NAND:8 bits width,with page size of 512B, 4 Address cycles support per page, using MPP multiplexing option of NAND 8 bits
0X0A	BootROM Enabled, Boot from NAND:8 bits width,with page size of 2KB, 4 bits ECC support per page, using MPP multiplexing option of NAND 8 bits
0X0B	BootROM Enabled, Boot from NAND:8 bits width,with page size of 2KB, 8 bits ECC support per page, using MPP multiplexing option of NAND 8 bits
0X0E	BootROM Enabled, Boot from NAND:8 bits width,with page size of 4KB, 4 bits ECC support per page, using MPP multiplexing option of NAND 8 bits
0X0F	BootROM Enabled, Boot from NAND:8 bits width,with page size of 4KB, 8 bits ECC support per page, using MPP multiplexing option of NAND 8 bits
0X18	BootROM Enabled, Boot from NAND: 16bits width,with page size of 512B, 3 Address Cycles support per page, using MPP multiplexing option of NAND 16 bits
0X19	BootROM Enabled, Boot from NAND: 16bits width,with page size of 512B, 4 Address Cycles support per page, using MPP multiplexing option of NAND 16 bits
0X1A	BootROM Enabled, Boot from NAND: 16 bits width,with page size of 2KB, 4 bits ECC support per page, using MPP multiplexing option of NAND 16 bits
0X1B	BootROM Enabled, Boot from NAND: 16 bits width,with page size of 2KB, 8 bits ECC support per page, using MPP multiplexing option of NAND 16 bits
0X1E	BootROM Enabled, Boot from NAND: 16 bits width,with page size of 4KB, 4 bits ECC support per page, using MPP multiplexing option of NAND 16 bits
0X1F	BootROM Enabled, Boot from NAND: 16 bits width,with page size of 4KB, 8 bits ECC support per page, using MPP multiplexing option of NAND 16 bits
0X26	BootROM Enabled, Boot from SPI: Controller #0. NAND Flash type, using MPP multiplexing option of SPI on MPP [25:22]
0X27	BootROM Enabled, Boot from SPI: Controller # 1. NAND Flash type, using MPP multiplexing option of SPI on MPP [59:56]
0X28	BootROM Enabled, Boot from UART: Controller # 0. supporting Boot, using MPP multiplexing option of UART on MPP [1:0]
0X2A	BootROM Enabled, Boot from SATA0: Controller # 0. using SERDERS multiplexing option of SATA on Lane # 0

0X2B	BootROM Enabled, Boot from SATA0: Controller # 0. using SERDERS multiplexing option of SATA on Lane # 1
0X2C	BootROM Enabled, Boot from PCIe0: Controller # 0. using SERDERS multiplexing option of PCLe on Lane # 0
0X2D	BootROM Enabled, Boot from PCIe0: Controller # 0. using SERDERS multiplexing option of PCLe on Lane #1
0X30	BootROM Enabled, Boot from SDIO: Controller #0. using MPP multiplexing option of SDIO on {MPP [59:57], MP[55:52], MPP[50:48]}
0X31	BootROM Enabled, Boot from SDIO: Controller #0. using MPP multiplexing option of SDIO on {MPP [40:37], MPP[28:24], MPP[21]}
0X32	BootROM Enabled, Boot from SPI: Controller #0. 24 address bits, NOR Flash type using MPP multiplexing option of SPI on MPP [25:22]
0X33	BootROM Enabled, Boot from SPI: Controller #0. 32 address bits, NOR Flash type using MPP multiplexing option of SPI on MPP [25:22]
0X34	BootROM Enabled, Boot from SPI: Controller # 1. 24 address bits, NOR Flash type using MPP multiplexing option of SPI on MPP [59:56]
0X35	BootROM Enabled, Boot from SPI: Controller # 1. 32address bits, NOR Flash type using MPP multiplexing option of SPI on MPP [59:56]
0X36	Reversed
0X38	Reversed

CPU Speed setting

Following are the defined values. All other values are reserved:

Setting	**Details**
0x0	Processor speed of 666MHz
0x2	Processor speed of 800MHz
0x4	Processor speed of 1066MHz
0x6	Processor speed of 1200MHz
0x8	Processor speed of 1333MHz
0xC	Processor speed of 1600MHz

We run our boards at 1600MHz. Industrial devices are limited to 1333MHz.
DRAM runs at half the Processor speed.

Mechanical and layout design

TBD

Refer to SDIO interface trace length matching.

Appendix A – A38x-uSoM Board-to-Board pinout.

A38x MicroSoM
Pinout.xlsx