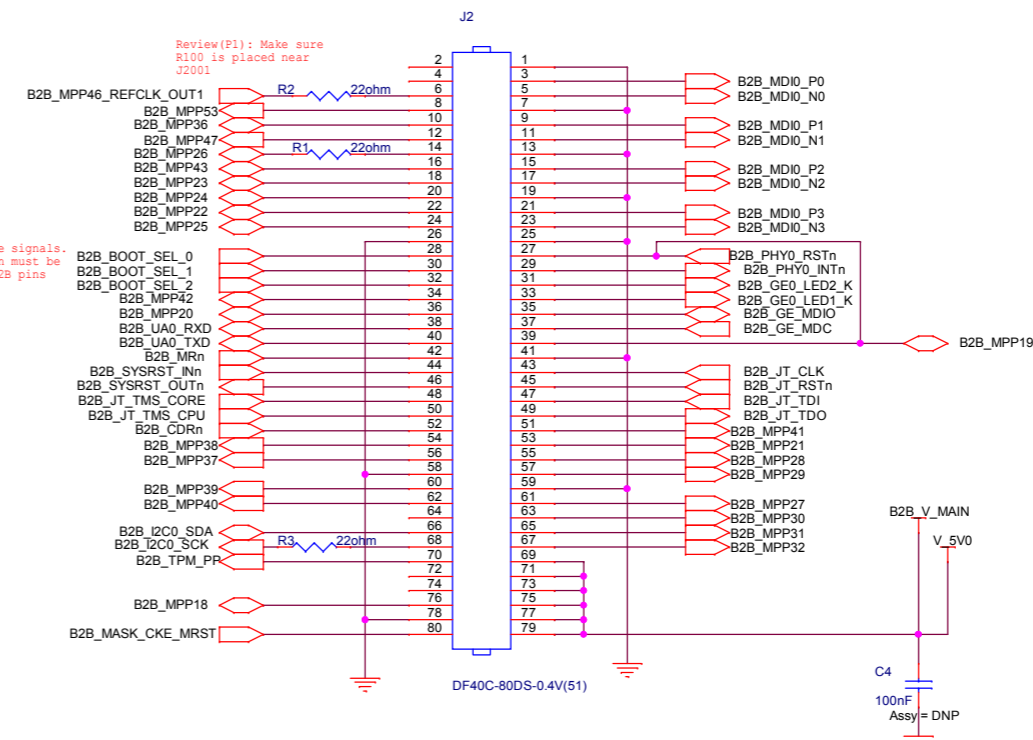
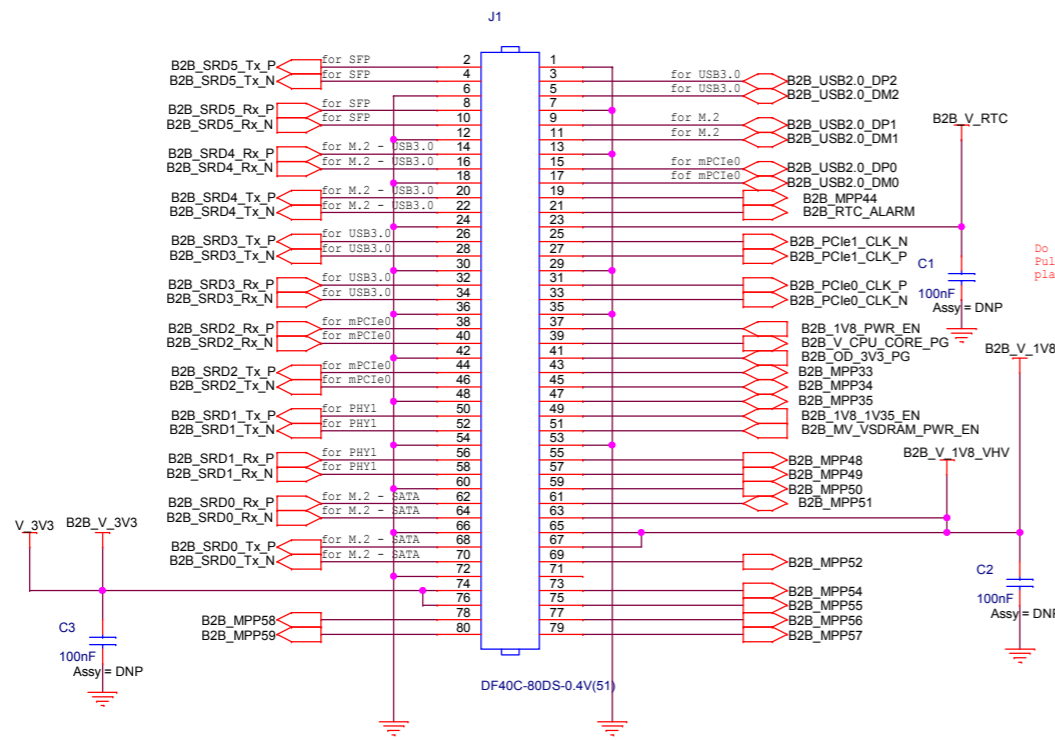


To Extract BOM:

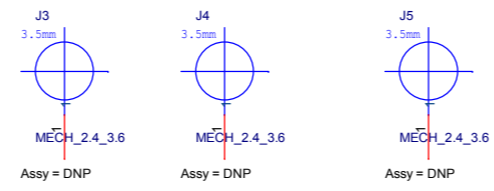
Item\tQuantity\tAssemblyOption\tPart\tPCB Footprint\tDescription\tDataSheet\tManufacturer\tManufacturer P/N\tSolidRun P/N\tReference
{Item}\t{Quantity}\t{ASSY}\t{Value}\t{PCB Footprint}\t{DESCRIPTION}\t{Datasheet}\t{Manufacturer}\t{Manufacturer P/N}\t{SolidRun P/N}\t{Reference}

To Extract BOM:

Item\tQuantity\tAssemblyOption\tValue\tDescription\tManufacturer Name\tManufacturer P/N\tSolidRun P/N\tPCB Footprint\tReference
{Item}\t{Quantity}\t{Assy}\t{Value}\t{DESCRIPTION}\t{Manufacturer Name}\t{Manufacturer P/N}\t{SolidRun P/N}\t{PCB Footprint}\t{Reference}

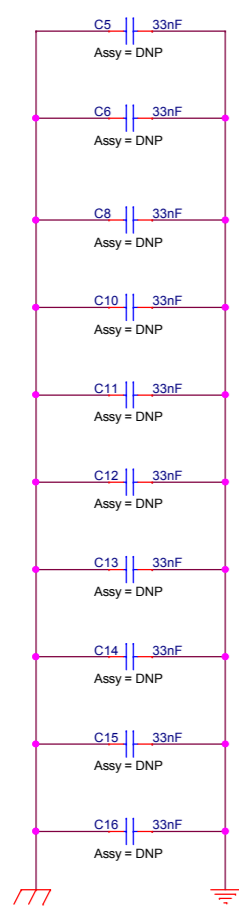


Four mechanical holes for the MicroSoM

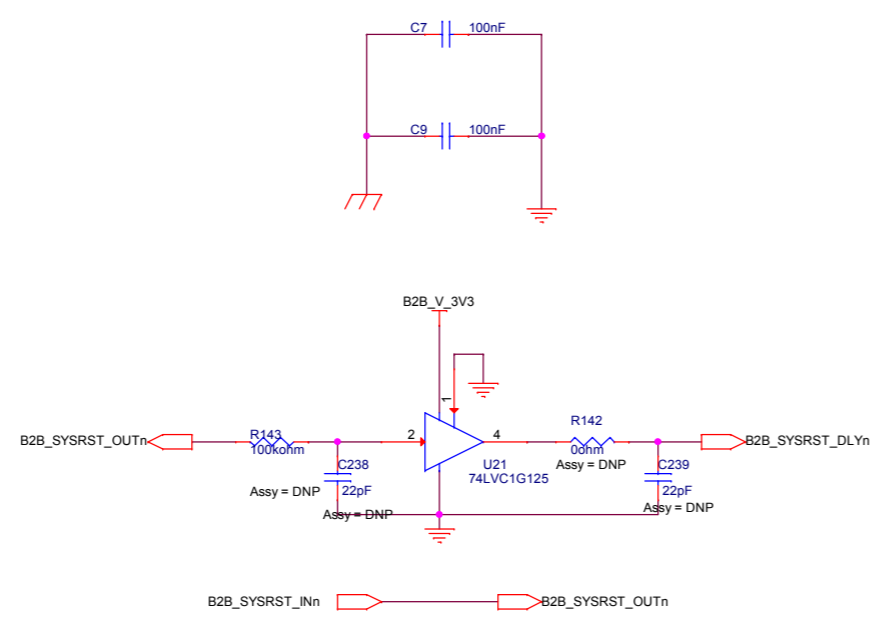


4th mechanical hole was removed due to routing limitations

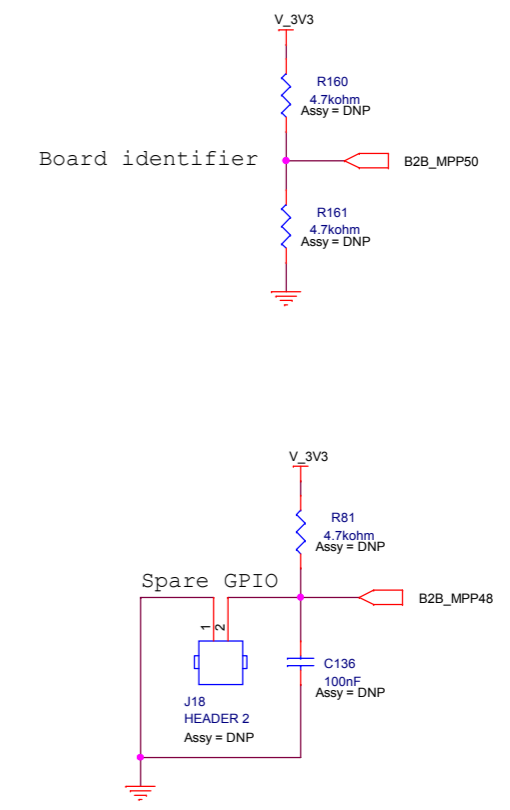
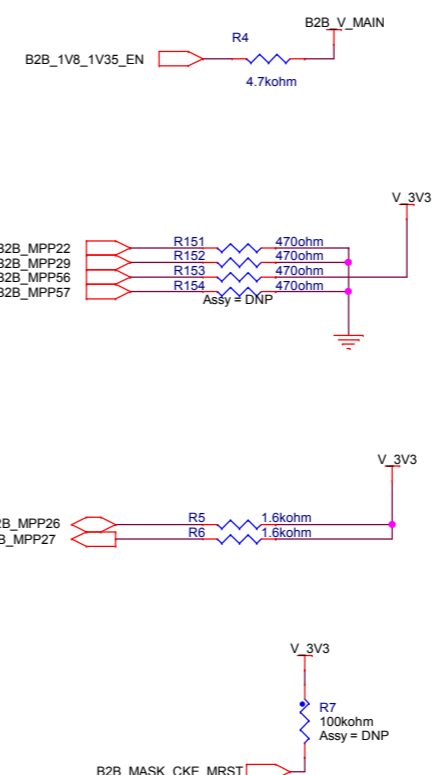
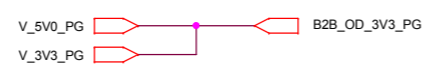
Bypass capacitors between GNDC and GND

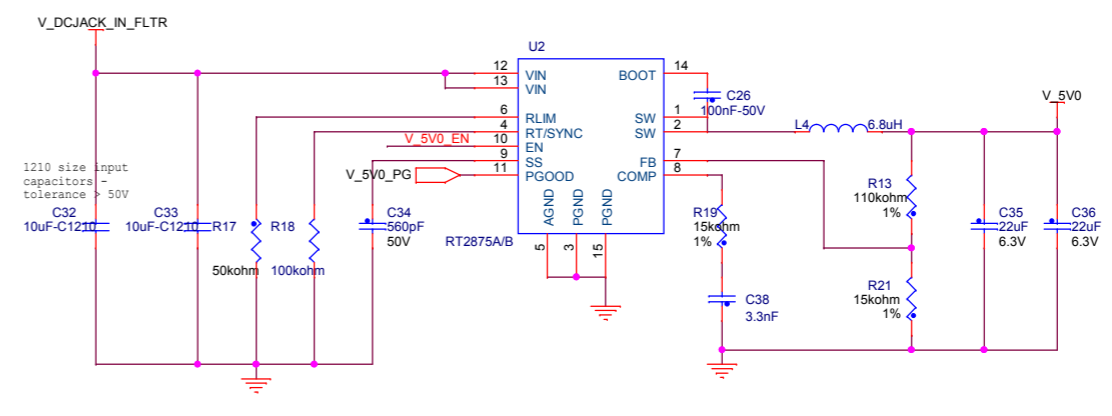
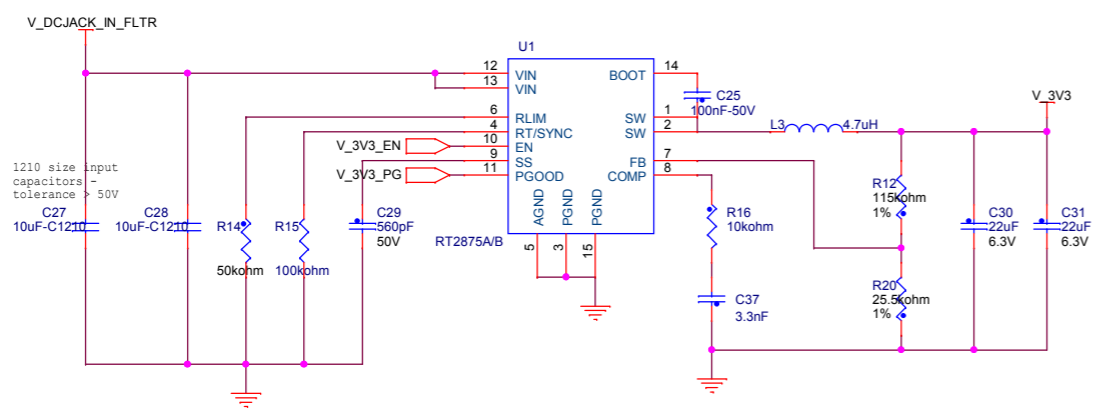
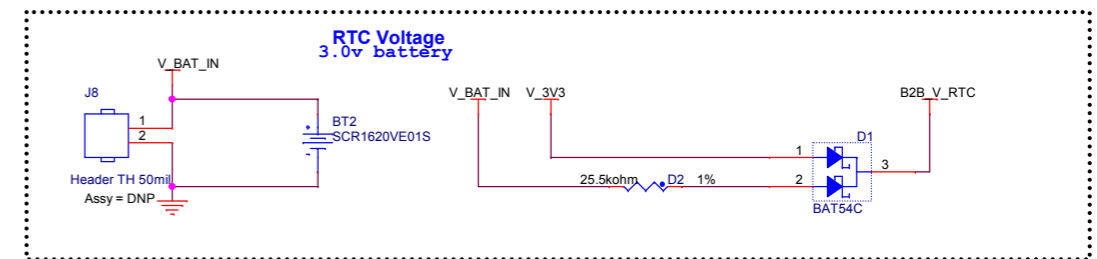
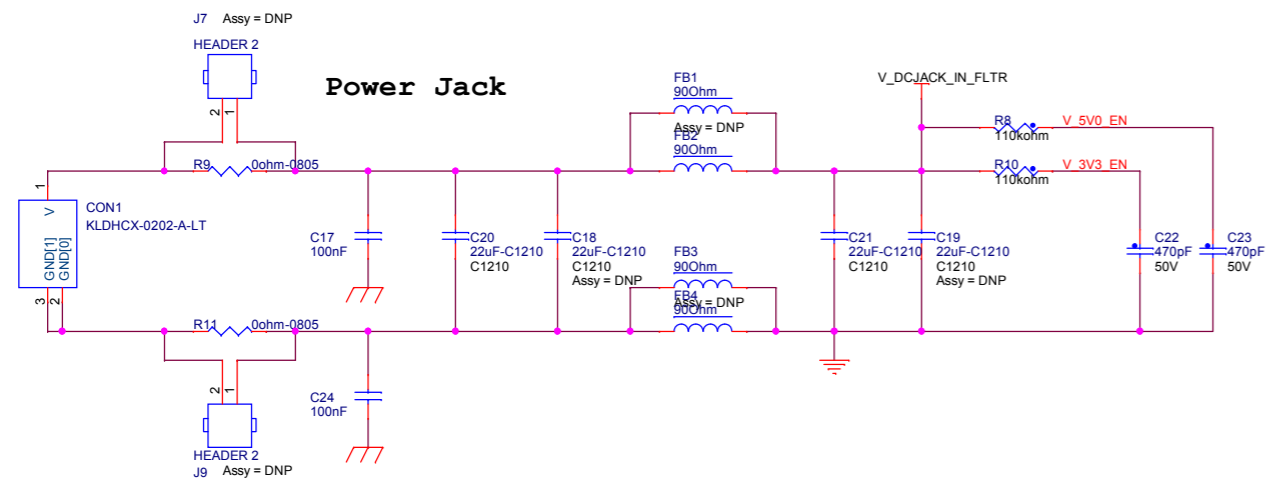


Bypass capacitors for MDIO passing underneath GNDC

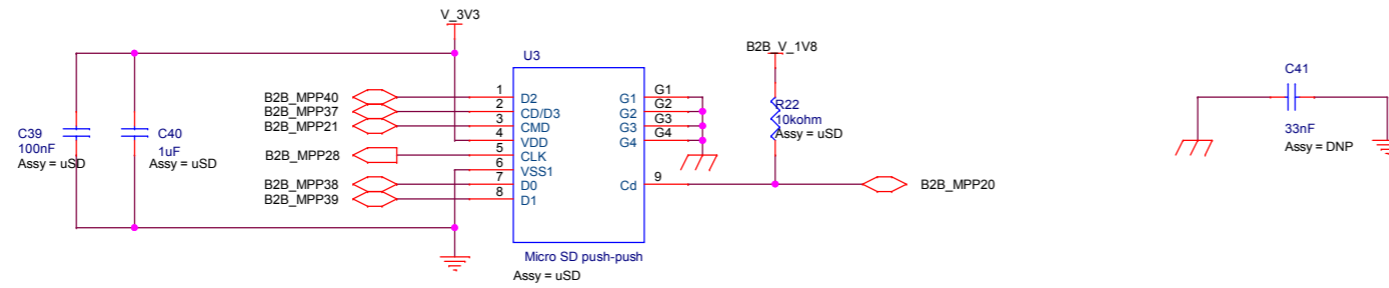


Carrier DC-DC PGOOD Signals will enable CPU DC-DC on uSoM. Signal is pulled up on uSoM.



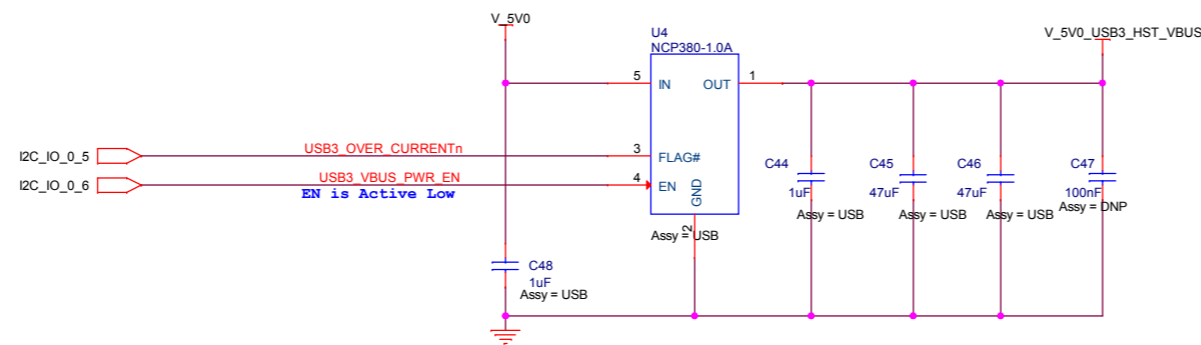
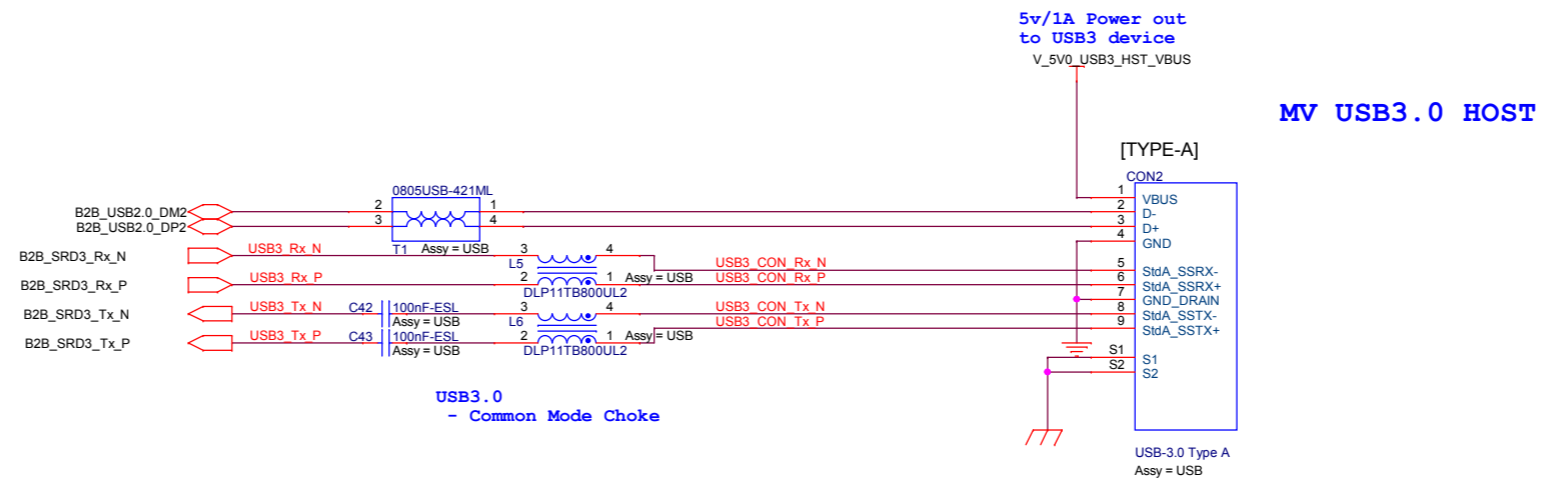


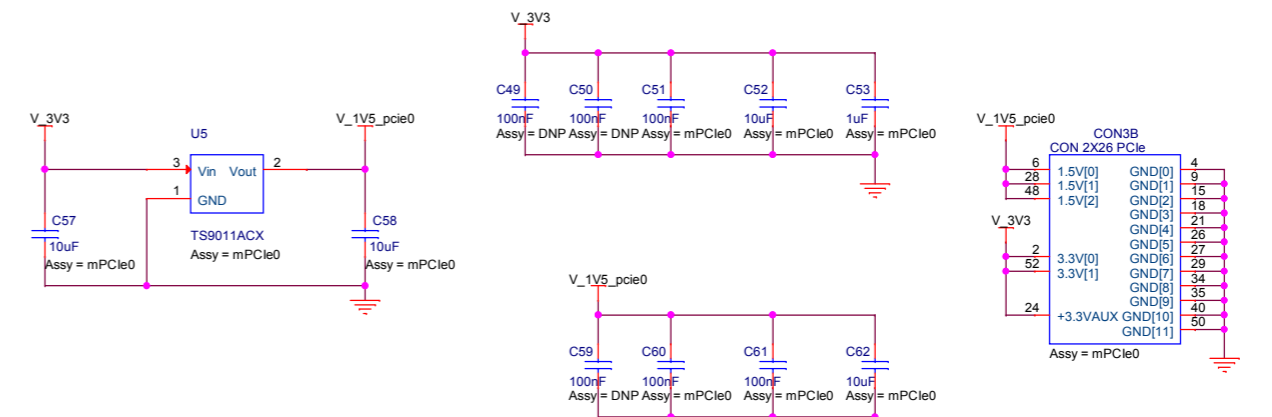
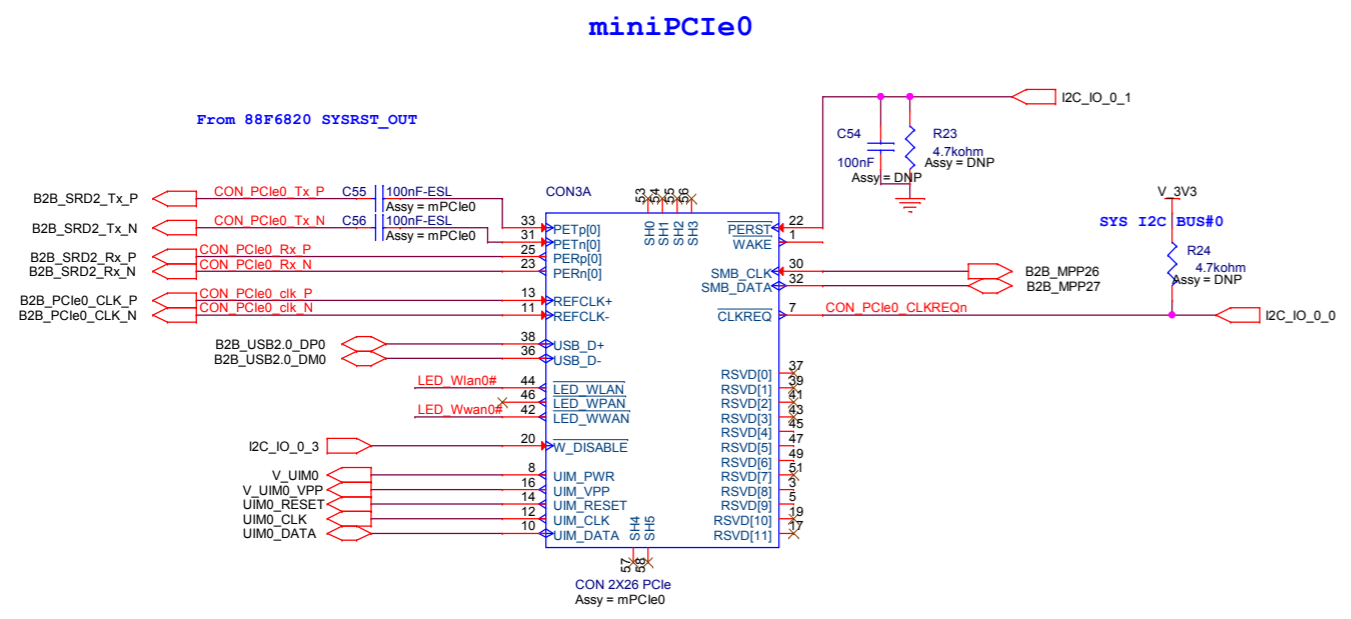
uSD



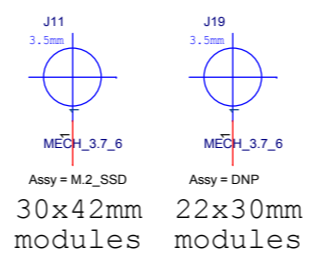
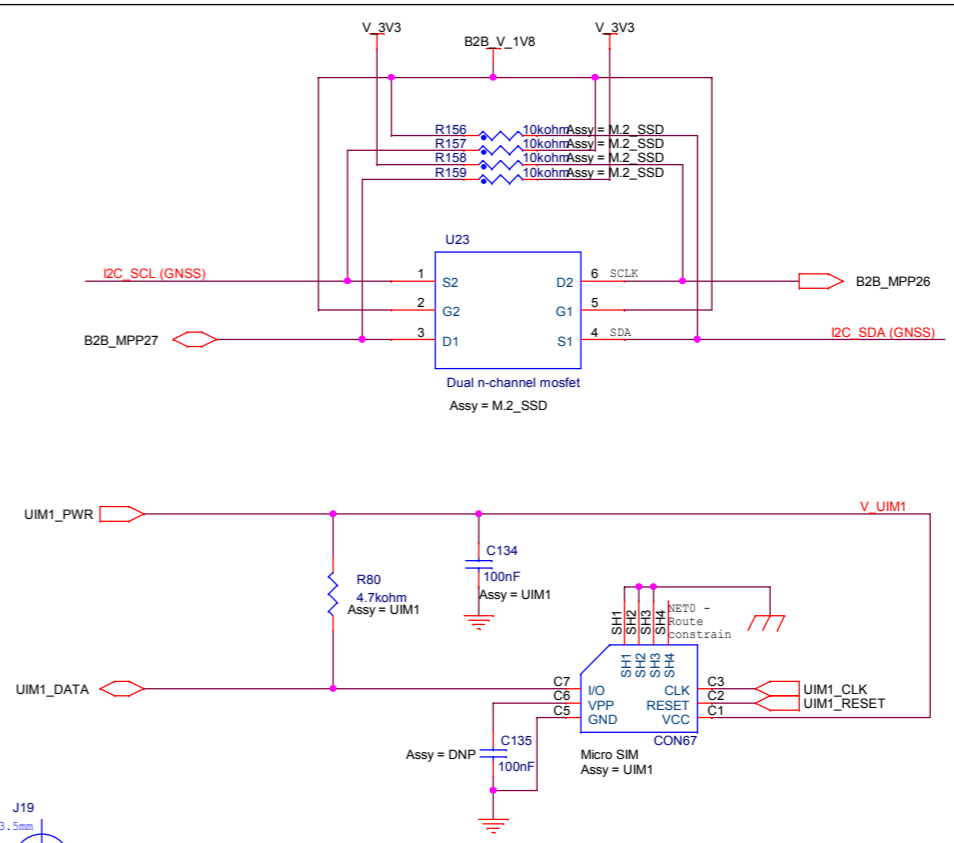
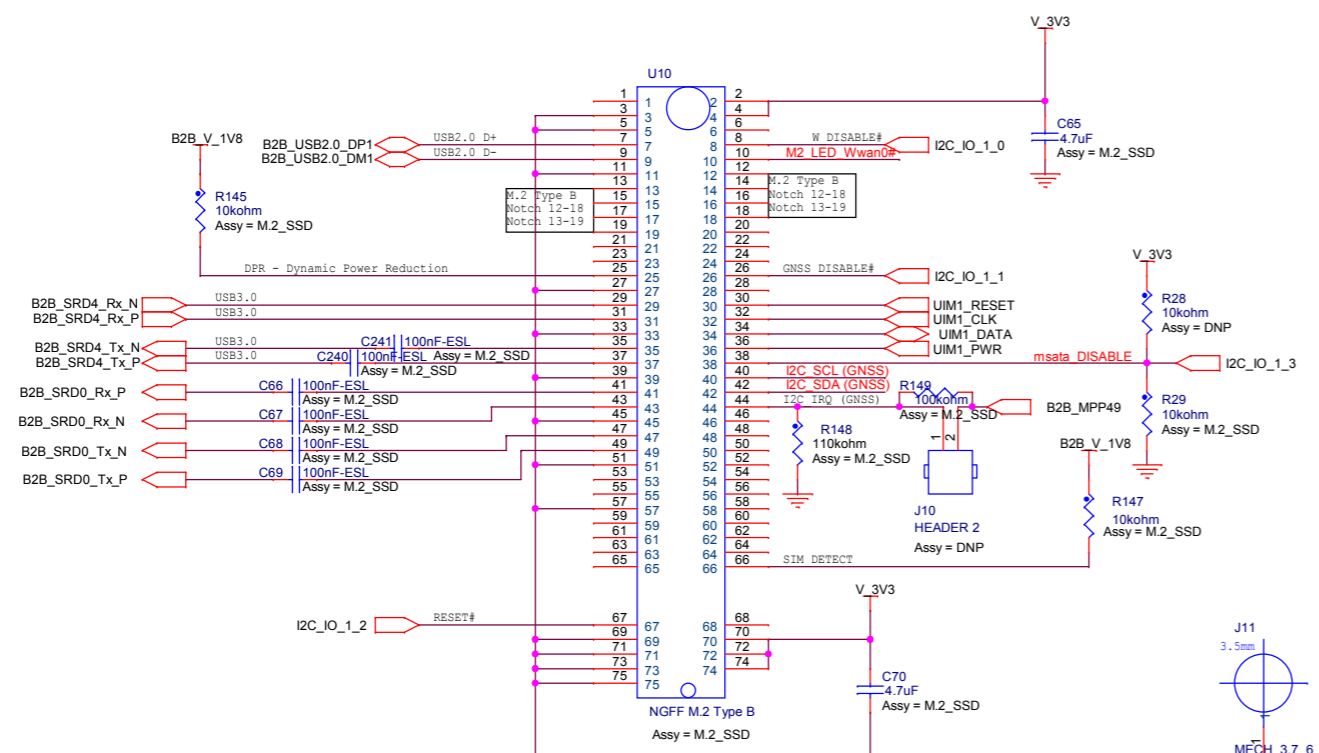
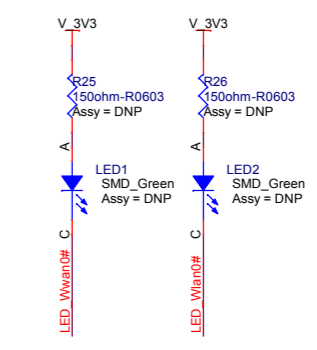
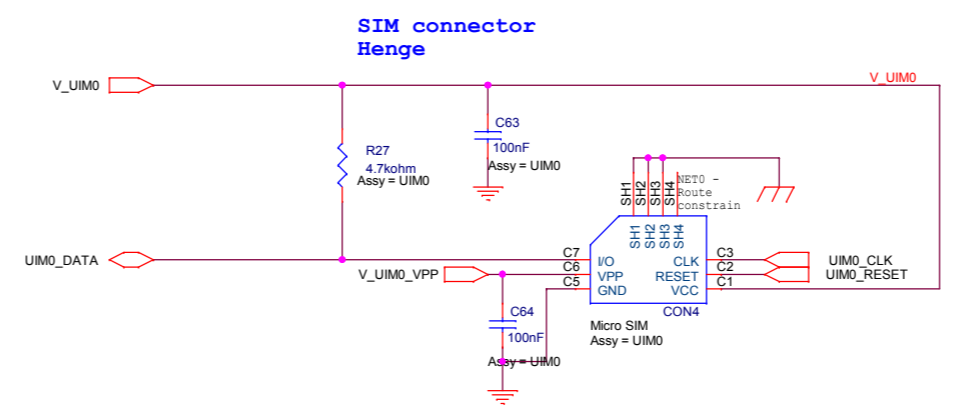
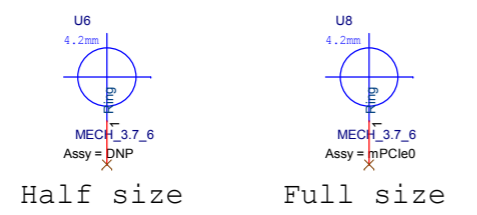
USB2.0
- Common Mode Choke

Connector side

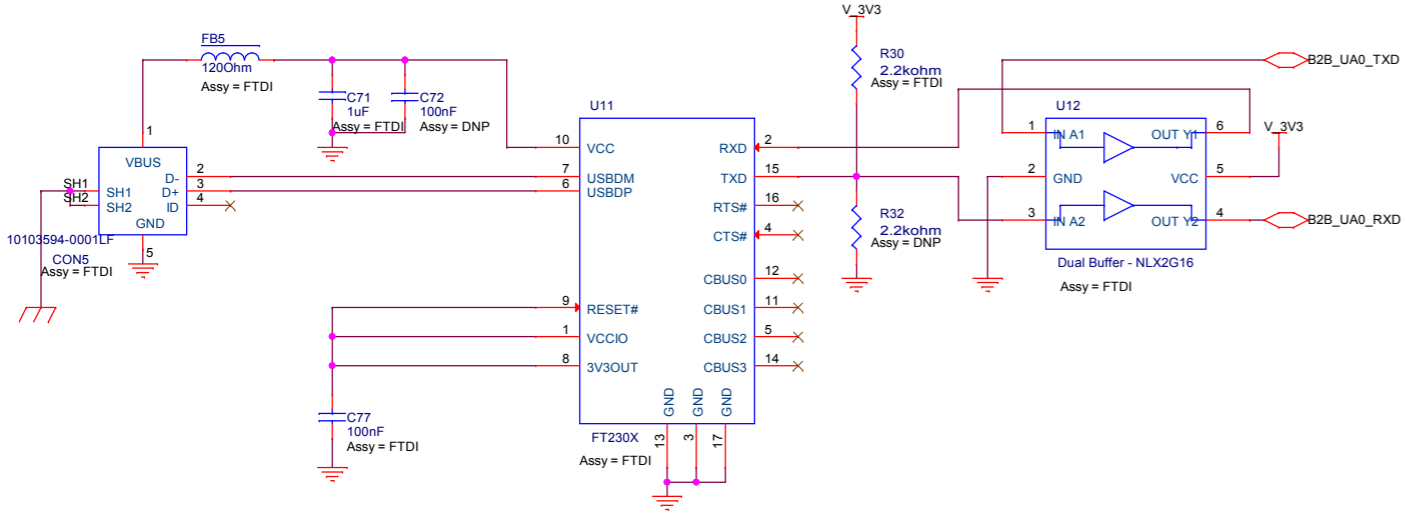




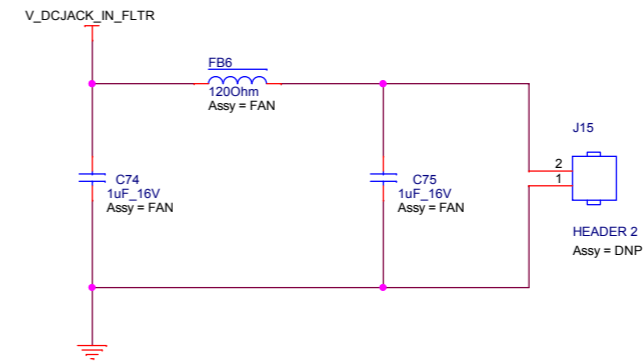
Mechanical holes/spacers for the mPCIe module



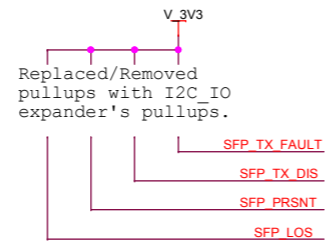
microUSB to UART



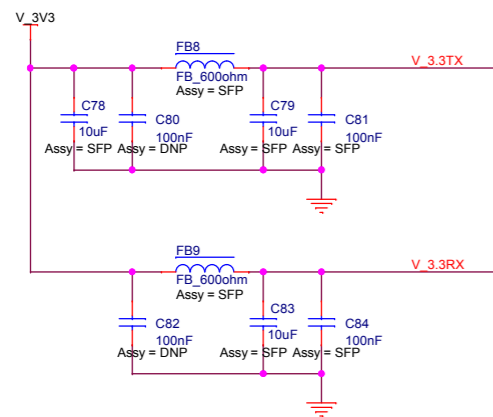
FAN Power



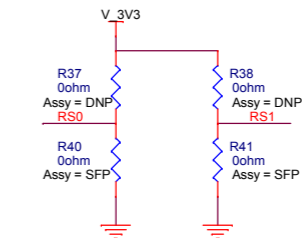
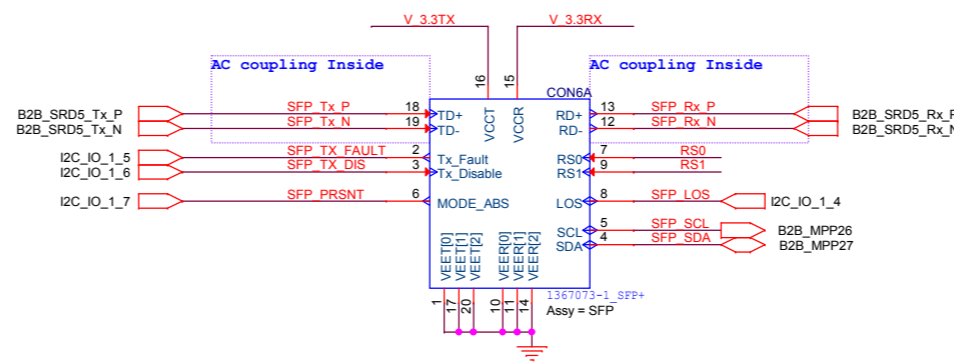
SFP + defines maximum current withdraw from V_3.3TX and V_3.3RX as 300mA each.



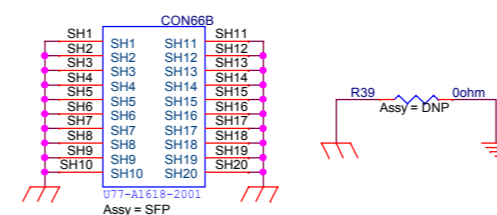
SFP TRANSCEIVER Power



SFP TRANSCEIVER

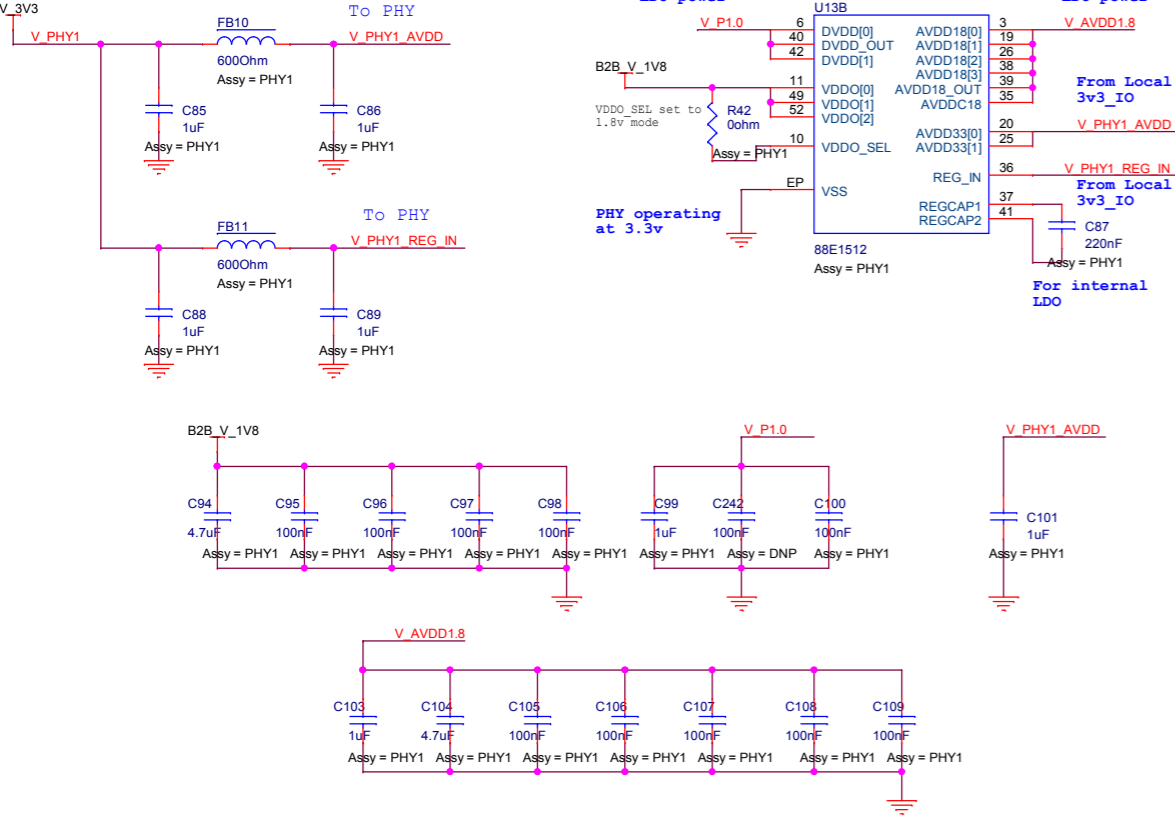


SFP Shield



PHY Power configurations

88E1512 power configurations:
 1. using internal lv8 and lv0 regulators.
 2. VDDO_SEL config VDDO to operate at 2v5/3v3.



PHYADD configuration

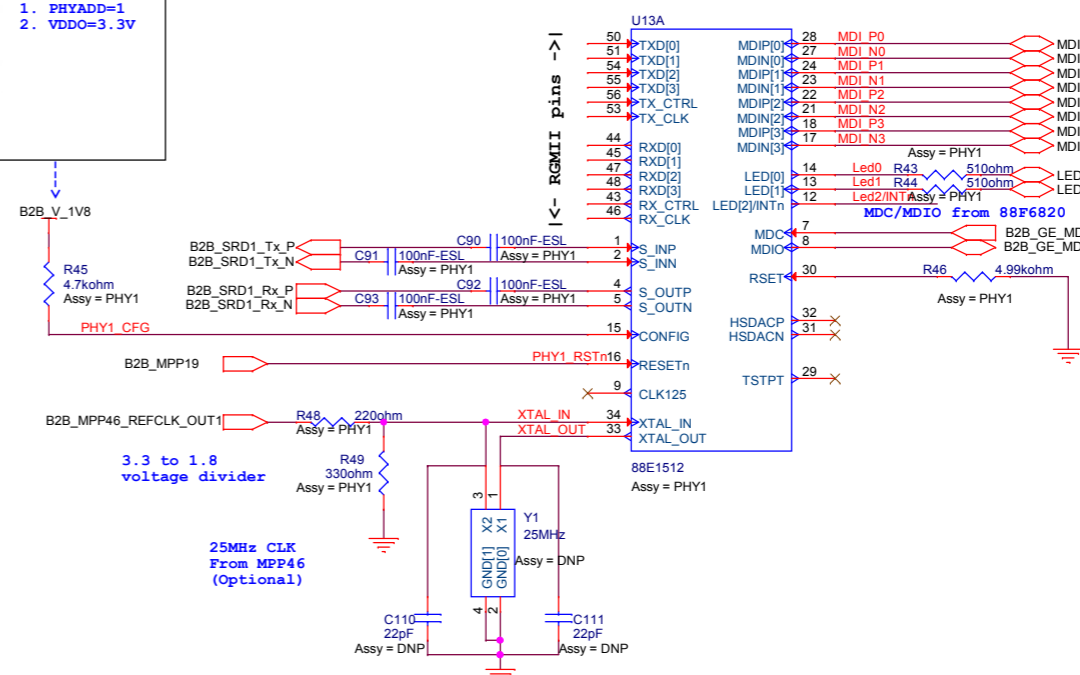
88E1512 PHY configuration options:
PHY_address=1

Pin	CONFIG Bit1	CONFIG Bit 0	Value Assignment
CONFIG 0	0	0	PHYADD[0] = 0 VDDO_LEVEL ¹ = 3.3V
CONFIG 1	1	1	PHYADD[0] = 1 VDDO_LEVEL ¹ = 3.3V
CONFIG 1	0	0	PHYADD[0] = 0 VDDO_LEVEL ¹ = 2.5V
CONFIG 0	1	1	PHYADD[0] = 1 VDDO_LEVEL ¹ = 2.5V

¹. This is valid only for 88E1510/88E1512. For 88E1518, the VDDO_LEVEL is fixed at 1.8V, hence the bit mapping for VDDO_LEVEL is ignored.

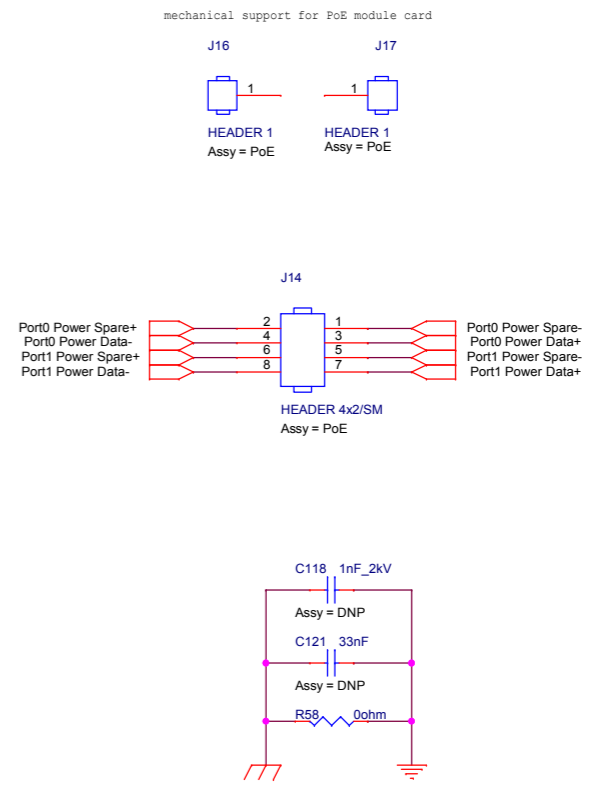
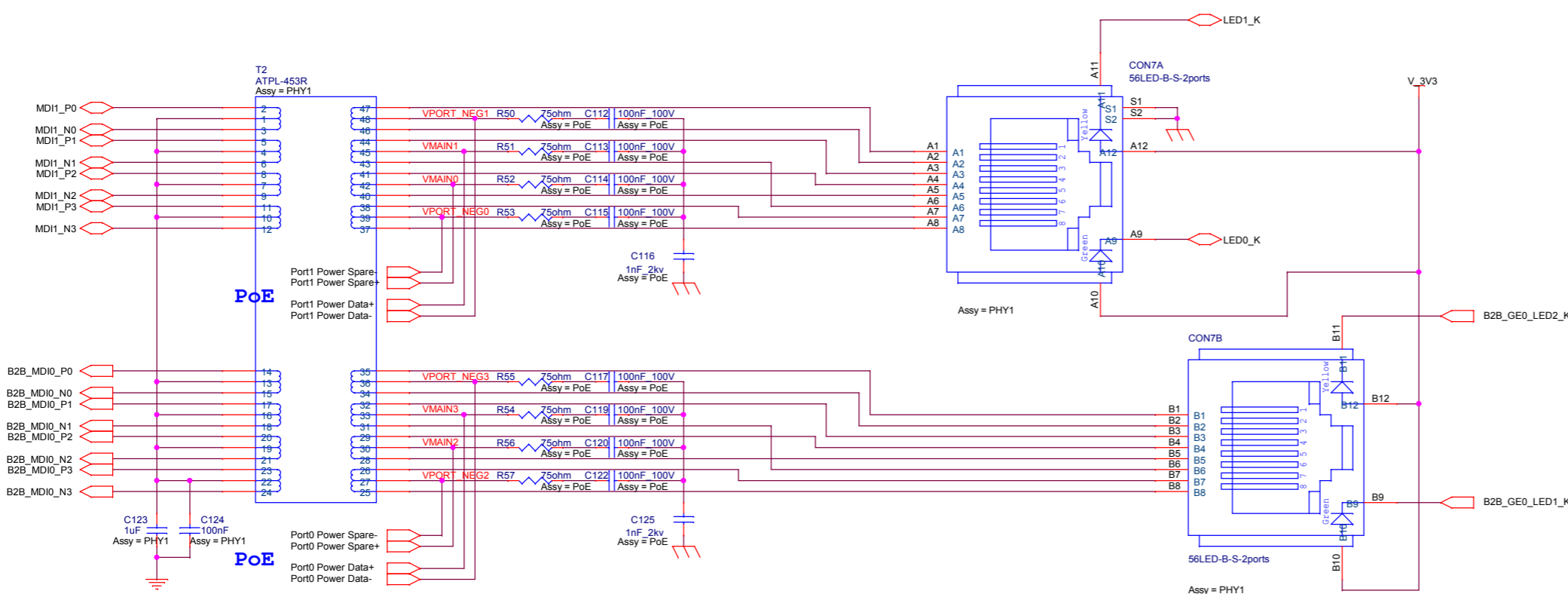
- 1. PHYADD=1
- 2. VDDO=3.3V

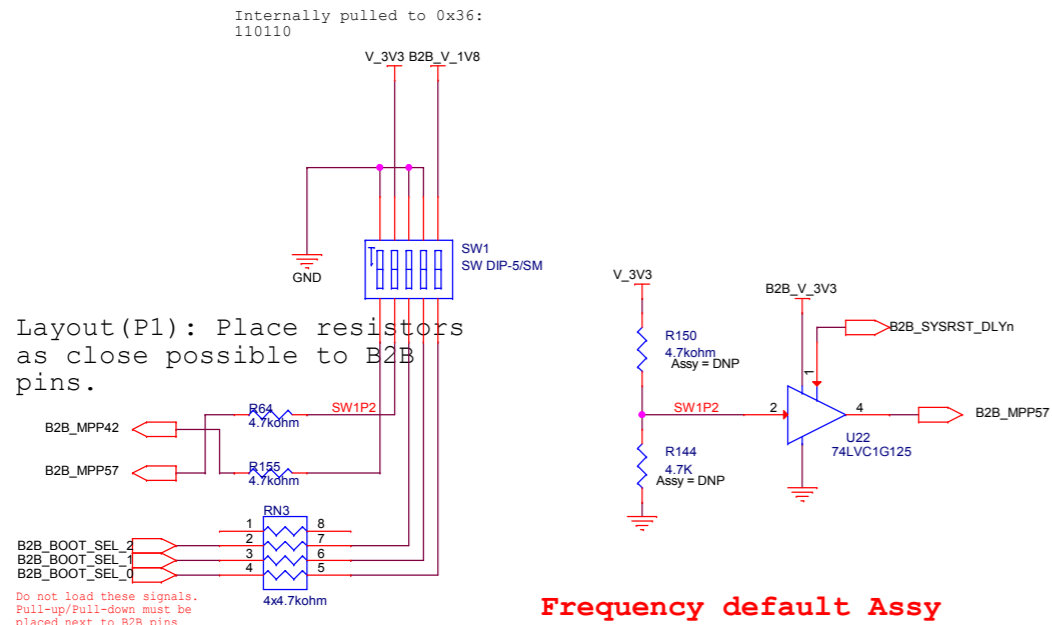
PHY1 - SGMII1 Function as GE1 Port



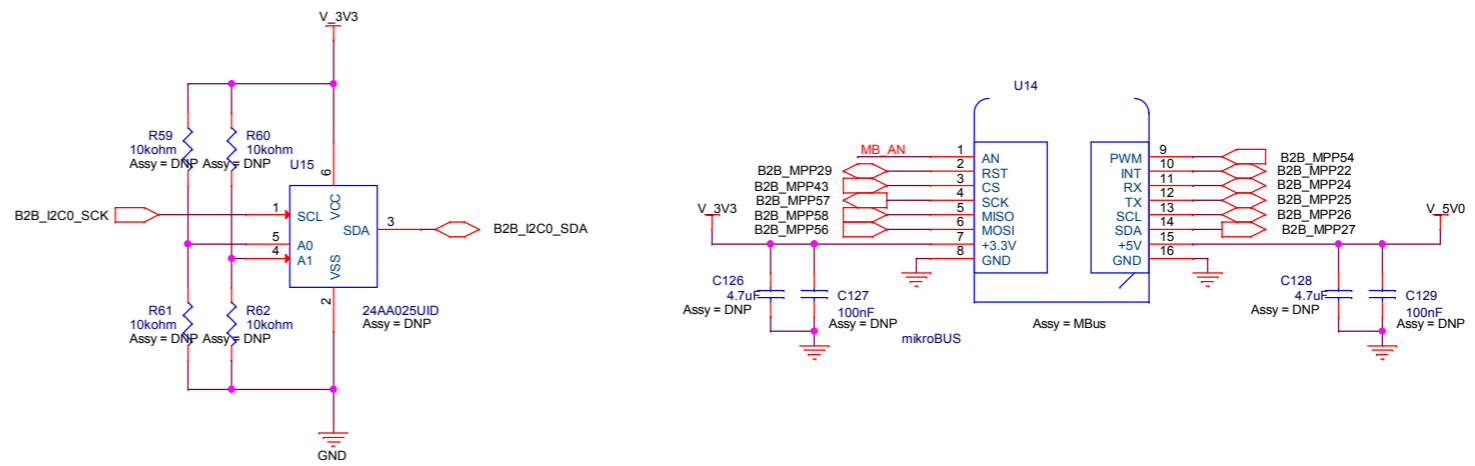
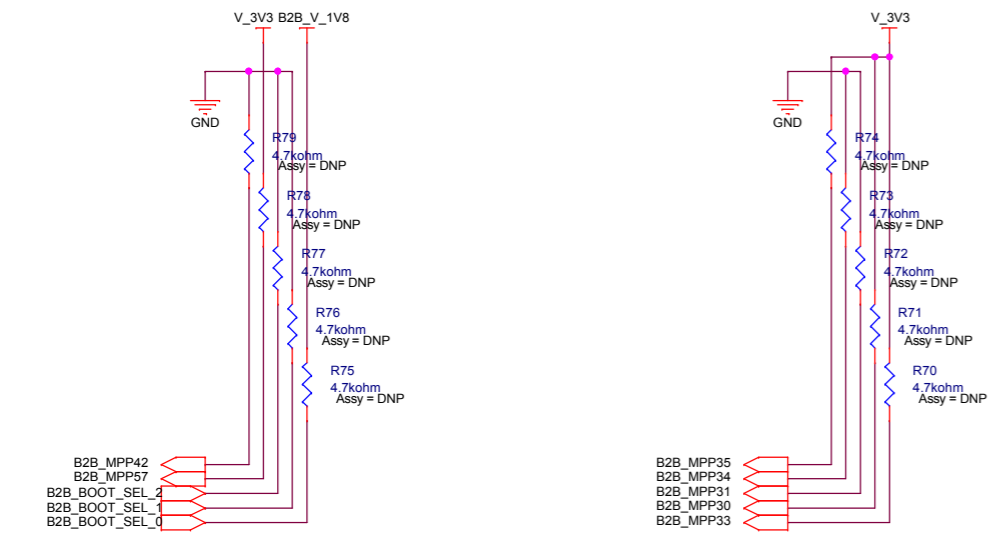
3.3 to 1.8 voltage divider

25MHz CLK From MPP46 (Optional)





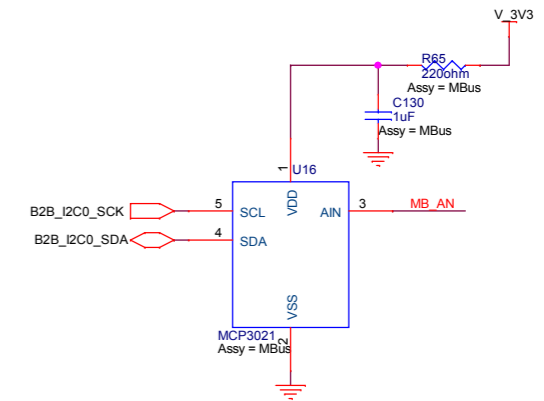
Frequency default Assy



PART NO.	XX	X	XX	
Device	Address Options	Temperature Range	Package	
Device: MCP3021T: 10-Bit 2-Wire Serial A/D Converter (Tape and Reel)				
Temperature Range: E = -40°C to +125°C				
Address Options:				
	XX	A2	A1	A0
A0	= 0	0	0	
A1	= 0	0	1	
A2	= 0	1	0	
A3	= 0	1	1	
A4	= 1	0	0	
A5*	= 1	0	1	
A6	= 1	1	0	
A7	= 1	1	1	
* Default option. Contact Microchip factory for other address options				
Package: OT = SOT-23, 5-lead (Tape and Reel)				

Examples:

- MCP3021A0T-E/OT: Extended, A0 Address, Tape and Reel
- MCP3021A1T-E/OT: Extended, A1 Address, Tape and Reel
- MCP3021A2T-E/OT: Extended, A2 Address, Tape and Reel
- MCP3021A3T-E/OT: Extended, A3 Address, Tape and Reel
- MCP3021A4T-E/OT: Extended, A4 Address, Tape and Reel
- MCP3021A5T-E/OT: Extended, A5 Address, Tape and Reel
- MCP3021A6T-E/OT: Extended, A6 Address, Tape and Reel
- MCP3021A7T-IE/OT: Extended, A7 Address, Tape and Reel



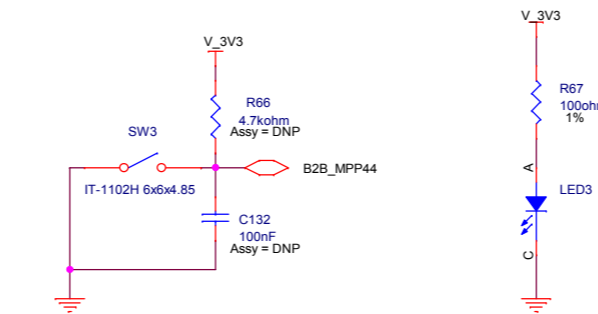
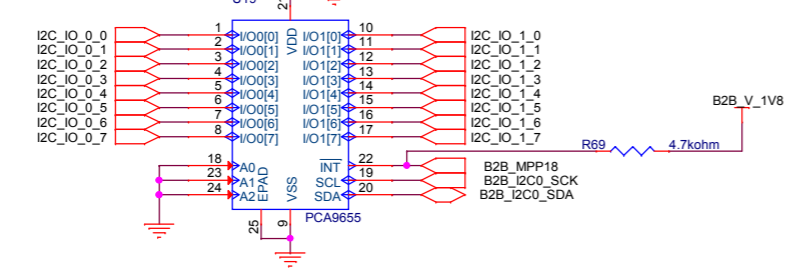
PCA9555
16-bit I2C and SMBus I/O port with interrupt
5V tolerant I/Os

I/O port
When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high impedance input with a weak pull-up to VDD. The input voltage may be raised above VDD to a maximum of 5.5 V

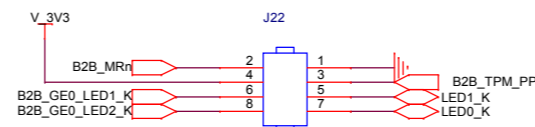
I/O Table

I02_0
I02_1
I02_2
I02_3
I02_4
I02_5
I02_6
I02_7
I03_0
I03_1
I03_2
I03_3
I03_4
I03_5
I03_6
I03_7

I2C Add: 0x21



AP Reset Switch (GPIO)



RJ-45 LEDs, Board Reset and TPM_PP

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